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(54) A method and an arrangement for adapting the rate at which data information is read from a memory to the rate at which data information is written into the memory.

(57) The present invention relates to the technical field of memory storage and digital teletransmission, and more particularly to a method and to an arrangement for writing data into a memory (FIFO) and reading data therefrom such that the read-out rate is, on average, as high as the write-in rate. The incoming frames ($Data_{in}$) to the memory include datainformation ($DATAINFO_{in}$) and other information (OTHER) . Only the datainformation is to be written into the memory. A write address generator (RADRGEN) generates a cyclic sequence of write addresses for each occurrent datainformation unit to be written into the memory. A cyclic sequence of read addresses is generated in a read address generator (WADRGEN) for reading information from the memory. The arrangement also includes a phase-locking circuit (PLL) which functions to adjust the read-out rate, by adjusting the rate at which read addresses are generated. According to the invention, means are provided for detecting whether a frame incoming to the memory (FIFO) contains more or fewer datainformation units than the nominal number. If the frame contains more or fewer datainformation units, this is masked initially for the phase-locking circuit, by changing a first reference address (a) so that the phase-locking circuit (PLL) will not change momentarily the rate at which the read addresses are generated. The mask is then removed in incremental steps, whereby the phase-locking circuit adjusts the rate at which read addresses are generated stepwise, i.e. the read-out rate. This prevents the phase-locking circuit from rapidly carrying out very large rate changes.

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TECHNICAL FIELD

The present invention relates to the technical field of memory storage and digital teletransmission. More particularly, the invention relates to a method and to an arrangement of apparatus for writing data into a memory and for reading data therefrom in a manner such that the read-out rate will, on average, be equally as high as the data write-in rate. The invention also relates to a method and means for transmitting data information between synchronous and plesisochronous digital hierarchy systems, in which data from one system is written into a memory and data intended for the other system is read-out from said memory.

BACKGROUND ART

In known techniques, different types of phase locking circuits PLL are used to control the memory read-out rate in a manner such that data will be read from the memory at a rate which is as high as the rate at which data is written into the memory.

For instance, in known techniques phase locking circuits are used to control the memory read-out rate when the write-in rate varies as a result of deficiencies in the transmission system. Phase locking circuits are also used to control the read-out rate of data in those instances when writing of data into the memory is repeatedly interrupted. One example of how a phase locking circuit is used is disclosed in U.S. Patent Specification U.S. 4,941,156.

In certain novel types of digital transmission systems, data information is transmitted from a synchronous digital hierarchy system (SDH) to a plesiochronous digital hierarchy system (PDH) via an addressable memory. The data information is divided on frames in the synchronous digital system. These frames include units of data information which are to be transmitted to the PDH-system, and also units of other information which shall not be transmitted. The number of data information units can vary with different frames, as a result of adjustments and justifications made in conjunction with the transmission of data between different SDH-systems. These variations are such as to cause the number of data information units to deviate from a nominal number of data information units in a predetermined manner. When transmitting data information from an SDH-system to a PDH-system, data information is written into an addressable memory, and since the number of data information units may be different in different frames, the information write-in rate is liable to vary. Data information written into the adressable memory is read therefrom into the PDH-system, and when reading data from the memory it is necessary to regulate the read-out rate so that it will be, on average, equally as high as the rate at which information is written into the memory, so that the memory will not become overfilled with data or empty of data. A write counter is used to indicate the address at which data shall be written into the memory, and a read counter is used to indicate the address from which data shall be read from the memory. In practice, the read-out rate is therefore controlled by controlling the rate at which read addresses are generated.

The problem arising with the use of a phase locking circuit to regulate the memory read-out rate when transferring data information from an SDH-system to a PDH-system in accordance with known techniques, is that jitter occurs on the output of the addressable memory. Jitter is caused because the variations in the number of units per frame in the SDH-system is, relatively speaking, so large and occurs so seldomly that the phase locking circuit is unable to regulate the read-out rate, but generates troublesome jitter which is propagated further in the transmission system.

Swedish Patent Application No. 9201672-4 discloses another type of arrangement for regulating the rate at which data is read from an addressable memory, this arrangement having the form of a buffer between an SDH-system and a PDH-system. In addition to the addressable memory, the buffer also includes a write counter which produces write addresses at the rate at which incoming data information enters the memory, and a read counter which produces read addresses from which data shall be read-out from the memory. The write-in rate may vary in response to the amount of datainformation contained in the frames, and the object of this arrangement is to control the read-out rate in a manner to follow the varying write-in rate. For the purpose of controlling data read-out rate, the arrangement includes a mean value counter which is operable to generate mean value addresses around which the write addresses pendulate. The generated mean value addresses thus form the mean values of the generated write addresses. The arrangement includes a first phase detector for comparison between a generated write address and a simultaneously generated mean value address. The generation of mean value addresses is hastened or delayed when the write address deviates excessively from the mean value address as a result of variations in the data write-in rate, so that the write addresses will constantly pendulate around the mean value addresses. The mean value counter utilizes a high frequency clock for generating successive mean value addresses. The frequency of the high frequency clock is higher than the frequency at which the write addresses are generated, so as to enable the generation of a new mean value address to be hastened or delayed in steps. The data read-out rate is regulated by means of a second phase detector, in which each read address gene-rated is compared with the simultaneously generated mean value address, this comparison showing whether or not the data read-out rate

is too high. If the read-out rate is too high, the generation of read addresses is stopped temporarily, so that the read-out rate will become as high as the write-in rate.

DISCLOSURE OF THE INVENTION

A new standard has been formulated in accordance with CCITT in respect of the earlier mentioned transmission systems comprising SDH-systems, PDH-systems and transitions therebetween, for systems which operate at the frequency 155 MHz. The new standard concerning the content of the frames has been designated G.703, G.707-709 and G.781-784 respectively. According to this standard, the frames in the SDH-system contain respectively data information and other information divided in words each consisting generally of eight bits. When transmitting between a SDH-system and a PDH-system, only the datainformation is transmitted, this datainformation being written in words into an addressable memory in which the datainformation is stored intermediately prior to being readout to the PDH-system. According to specifications in the new standard, the amount of datainformation contained in each frame in the SDH-system may correspond to a nominal number of words, or may contain three words more or three words less than the nominal number of words for each frame. Since the amount of datainformation will thus vary from frame to frame, the rate at which information is written into the memory will also vary.

Thus, in accordance with the aforedescribed new standard, the amount of datainformation contained in respective frames may vary between the frames. As beforementioned, this is because datainformation is also transmitted between different SDH-systems and it is necessary to equalize any rate differencies between signals in the various SDH-systems when transmitting data. Differencies in rates in mutually coacting SDH-systems are equalized in accordance with specifications in the new standard. According to this standard, the rates are equalized by adding to a frame or removing therefrom three words of datainformation in a predetermined manner.

When synchronizing the data read-out rate with the varying data write-in rate in accordance with the new standard, it is unsuitable to use a phase locking circuit in accordance with the known technique, since this will amplify the jitter problem. Neither is it possible to use an arrangement according to the aforementioned Swedish Patent Application No. 9201672-4, since the mean value counter of this arrangement operates at a frequency which is higher than the frequency at which incoming datainformation enters the memory. In the case of an SDH-system which operates in accordance with the new standard, the information contained in the incoming frames enters the addressable memory at a frequency of 155 MHz. However, since no higher frequency that the mean value counter could use is available, an arrangement which includes this mean value counter cannot be used.

The problem of adapting the rate at which data is read from an addressable memory to the varying rate at which information is read into the memory is, of course, not unique to the transmission of information between SDH-systems and PDH-systems, but is also found in other contexts.

An object of the present invention is to provide a method of controlling the rate at which information is read from an addressable memory so that this rate, on average, will be equally as high as the rate at which information is written into the memory, without causing troublesome jitter in the event of momentary changes in the write-in rate.

In simple terms, this object is achieved by the steps of detecting any momentary changes that may occur in the write-in rate, initially masking these detected changes, reducing the masking successively, and regulating or adjusting the read-out rate to the write-in rate, including any masking of changes.

An arrangement according to the present invention may include detecting means for establishing a change in the rate at which the write addresses are delivered to the memory, a first derivating means for deriving a first comparison magnitude from the write addresses and from a first reference address, a second derivating means for deriving a second comparison magnitude from the read addresses and from a second reference address. These comparison magnitudes are delivered to a control means for regulating the read-out rate in accordance with the relationship between the comparison magnitudes. The arrangement also includes activating means for activating the derivation of at least one of the comparison units to a predetermined extent which corresponds to the detected rate change, so as to initially mask the rate change for the control means. The activating means functions to reduce the influence of the derivation successively, so that the control means will adjust the read-out rate incrementally, i.e. stepwise, such that said rate will be equally as high as the data write-in rate.

The inventive embodiments of a method and an arrangement are primarily, but not exclusively, intended for use in conjunction with transitions or transmissions between SDH- and PDH-systems, wherein the addressable memory is included in a buffer between said systems. In the SDH-system, the datainformation is divided on frames, which include units of datainformation which is to be transmitted to the PDH-system and also units of other information which is not to be transmitted to the PDH-system. The number of datainformation units contained in each frame may vary from frame to frame, depending on whether the frame contains a nominal number of da-

tainformation units or more datainformation units or less datainformation units than said nominal number.

According to one embodiment of an inventive arrangement, when writing datainformation into the memory a write address generator may generate a write address for each unit of datainformation which is to be transmitted to the PDH-system via the memory. These write addresses are generated in cyclic sequences. When reading information from the memory, the read addresses may be generated in cyclic sequences in a read address generator. A phase locking circuit is operative to adjust the read-out rate, by adjusting the rate at which read addresses are generated. According to the invention, a change in the rate at which datainformation enters the memory is detected. When a rate change is detected, i.e. when the number of datainformation units in an incoming frame is more or less than the nominal number, a corresponding generation of more or less write addresses is initially masked for the phase locking circuit, so that said circuit will not momentarily change the rate at which the read addresses are generated. This mask is then removed successively, so as to provide the phase locking circuit incrementally with information to the effect that a change in the write-in rate has been detected and so that the phase locking circuit will adjust the rate at which read addresses are generated in a stepwise manner, i.e. incrementally. Consequently, it is not necessary for the phase locking circuit to quickly carry out very large rate changes, therewith avoiding the risk of troublesome jitter.

The prime advantage afforded by the invention is that the read-out rate being adjusted in steps, and therewith prevents the problem of jitter occurring. The arrangement is also relatively simple to implement and costs can be kept low, since the components used are of a conventional kind.

The invention will now be described in more detail with reference to exemplifying embodiments thereof and also with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates how datainformation is distributed on frames in the synchronous system and in the plesiochronous system respectively.

Figure 2 illustrates a known technique for writing datainformation into a memory and for reading datainformation therefrom.

Figure 3 illustrates addresses in an addressable memory.

Figure 4 illustrates an inventive arrangement.

Figures 5a-5c illustrate the cyclic generation of write addresses in three different cases.

Figure 6 illustrates cyclic generation of read addresses at varying rates.

Figure 7 illustrates the memory positions with associated addresses in the addressable memory in the inventive arrangement.

Figure 8 illustrates pulses from a first and a second derivating means included in the inventive arrangement.

Figures 9a and 9b illustrate the time shift between pulses delivered by the derivating means.

Figure 10 is a diagram which illustrates variations in a first reference address.

BEST MODE OF CARRYING OUT THE INVENTION

A preferred embodiment of a method and an arrangement according to the invention uses and includes respectively a memory, a buffer, between a synchronous digital hierarchy system, a so-called SDH-system, and a plesiochronous digital hierarchy system, a so-called PDH-system. The object of the invention is to transmit datainformation from the SDH-system to the PDH-system via the memory, in a manner such that the rate at which datainformation is read from the memory will, on average, be equally as high as the rate at which datainformation is written into the memory.

In the synchronous system, datainformation is divided on frames $Data_{in}$, as illustrated in Figure 1. The Figure solely shows one part of a frame $Data_{in}$, a so-called row, although in reality the frame is comprised of a further eight parts, so-called rows, although it is only that part of the frame $Data_{in}$ shown in Figure 1 that has essential significance to the invention. In the following description, the frame part $Data_{in}$ shown in Figure 1 will be treated as though it comprised the whole of the frame, since the remaining information in the frame has no significance with regard to the present invention. The frame $Data_{in}$ in the SDH-system includes units of datainformation $DATAINFO_{in}$ to be transmitted to the PDH-system, and also units of other information OTHER, which is not to be transmitted to the PDH-system. The information in the frames in the SDH-system occur at the frequency of 155 MHz. The datainformation may, for instance, be comprised of speech signals to be transmitted from one telephone subscriber to another. The other information which is not to be transmitted to the PDH-system may comprise control information, transmission messages and frame reading words, among other things for controlling the transmission of datainformation between the SDH-system and the PDH-system. The ratio of the number of datainformation units $DATAINFO_{in}$ and the number of other information units OTHER in each frame may vary dependending on whether or not the frame contains a nominal number of datainformation units or more or less datainformation units than the nominal number. The number of datainformation units $DATAINFO_{in}$ in each frame varies in the case of the illustrated em-

bodiment solely in accordance with the earlier described new standard for signals in SDH-systems. One unit in the frame is corresponded by a byte, one word, and a datainformation byte is transmitted over eight time slots. The information is divided into a total of two hundred and seventy bytes per frame, each byte including eight binary coded bits. In Figure 1a there is shown one frame $Data_{in}$ which contains a nominal number of datainformation units $DATAINFO_{in}$ and a nominal number of units containing other information OTHER. In the illustrated example, the frame includes two hundred and sixty-one bytes of datainformation and nine bytes of other information. In the case of frames which contain a nominal number of datainformation units in this way, the datainformation appears in the SDH-system at the nominal frequency of 140 MHz. In practice, other information OTHER may also be incorporated among the datainformation $DATAINFO_{in}$, although this has been ignored here in order to simplify the description. In Figure Ib there is shown a frame in which the number of datainformation units $DATAINFO_{in}$ is greater than the nominal number. In the case of the illustrated embodiment, the frame includes three bytes more datainformation than is nominal. In accordance with the new standard, the frame includes three spaces H3 which correspond to twenty-four time slots and which are used to transmit three bytes more datainformation than is nominal. Thus, the frame includes in total two hundred and sixty-four bytes of datainformation. In the frame illustrated in Figure 1b, the amount of other information OTHER will therewith be smaller than nominal and is corresponded by six bytes instead of nine bytes. In the case of frames which contain more datainformation units than is nominal in this way, the datainformation appears at a frequency which is higher than the nominal frequency. In Figure 1c there is shown a frame which contains fewer datainformation units $DATAINFO_{in}$ than is nominal. According to this example, the frame has three bytes less datainformation than is nominal. In accordance with the new standard, the frame includes three spaces 0 corresponding to twenty-four time slots which are not used to transmit datainformation. Thus, the frame includes in total two hundred and fifty-eight bytes of datainformation. The amount of other information OTHER in the frame of Figure Ic will therewith be greater than is nominal and will correspond to twelve bytes instead of nine bytes. In the case of frames which contain fewer datainformation units than is nominal in this way, the datainformation appears at a frequency which is lower than the nominal frequency. Thus, the amount of datainformation contained in the frames illustrated in Figures 1a-1c may vary from frame to frame, meaning that the rate at which datainformation is written into the addressable memory will also vary correspondingly. In Figure 1d there is shown a frame $Data_{out}$ which includes datainformation $DATAINFO_{out}$ which is read wordwise from the memory to the PDH-system. The frames $Data_{out}$, which solely contain datainformation, have different sizes in different applications and in different systems. Outgoing datainformation is read from the memory at a rate which, on average, corresponds to the data write-in rate.

Figure 2 illustrates a known arrangement for writing datainformation into a memory and for reading datainformation therefrom. The memory 10, which is an addressable memory, is comprised of a FIFO-register (First In First Out) which comprises forty-four memory positions, each of which is intended to store one word. The memory 10 has write address inputs 11 for receiving write addresses WADR generated in a write address counter 12, and also includes read address inputs 13 for receiving read addresses RADR generated in a read address counter 14. The memory is further provided with data inputs 15 for receiving datainformation $DATAINFO_{in}$ and data outputs 16 for delivering datainformation $DATAINFO_{out}$.

For the purpose of describing the operation of a known arrangement, it is assumed that the datainformation to be written into the memory appears in frames $Data_{in}$ of the kind described with reference to Figure 1. Frames $Data_{in}$ containing datainformation and other information arrive at an input 17 on a series/parallel converter 18, which delivers the information in words to the data inputs 19 on a Demapper 20. An output 21 on the Demapper circuit 20 in connected to an input 22 on the write address counter 12. The content of the frames $Data_{in}$ is decoded by the Demapper circuit 20, and a write signal pulse WCLP is delivered to the write address counter 12 for each byte of datainformation to be written into the memory FIFO, therewith to generate a new write address. One word of datainformation $DATAINFO_{in}$ is written into the memory at the momentary address contained in the write address counter. The write addresses WADR, and also the read addresses, are generated cyclicly, as illustrated in Figure 3. The addresses are generated in binary coded form at cyclicly repeated intervals. The memory has forty-four addresses which range from zero to forty-three and the addresses are binary coded in a manner such that at the transition between address twenty-one and address twenty-two, the most significant bits in the binary code will pass from zero to one, while at the transition between address forty-three and zero, the most significant bit in the binary code will pass from one to zero.

The known arrangement uses a phase locking circuit to control the read-out rate from the memory 10. This phase locking circuit includes a phase detector 23, a lowpass filter LP and a voltage controlled oscillator VCO. The phase detector 23 has a first input 24 on which there is received a first signal which may have either one of two levels, a high level or a low level. A second signal which can assume a high or a low

level in a corresponding manner is received on a second input 25. The phase detector 23 functions to detect the time difference between corresponding level changes, from low to high level, in the first and the second signal and produces on an output a time difference signal td relating to the detected time difference. The output of the phase detector 23 is connected to an input on the lowpass filter LP on which the time difference signal td is received. In the lowpass filter LP there is derived a mean time value from consecutively received time difference signals td. An output on the lowpass filter LP is connected to the voltage controlled oscillator VCO. The lowpass filter delivers a control signal CO to the voltage controlled oscillator VCO, which produces pulses cl on an output clock at a frequency which depends on the control signal CO. Thus, the voltage controlled oscillator VCO produces clock pulses cl which may vary in frequency. The clock pulses may vary about a nominal frequency which corresponds to the nominal frequency at which datainformation $DATAINFO_{In}$ appears in the SDH-system. The output on the voltage controlled oscillator VCO is connected to an input of a counter 26 which has an output connected to the read address counter 14. The clock pulses cl are delivered to the counter 26, which with each eight clock pulses received delivers a read clock puls RCLP to the read address counter 14 for reading-out one word from the address disclosed by the counter content of the read counter 14.

The first input 24 on the phase detector 23 is connected to the output of an inverting circuit 27, which has an input connected to the most significant bit msb_{wa} on write addresses WADR delivered to the memory 10. The second input 25 is connected directly to the most significant bit msb_{ra} on read addresses RADR delivered to the memory 10.

The aforedescribed known arrangement with which datainformation is written into and read from a memory in a manner such that the read-out rate is, on average, equally as high as the write-in rate operates in the following manner. In a normal state, the write addresses WADR are generated with a shift from the read addresses RADR of one half address cycle, or are shifted from the read addresses as far as possible. This shift is desirable in order for the margins to be as wide as possible, so as to obviate the risk of data being written into and read from one and the same memory position simultaneously when the write-in rate changes. When the write address zero is generated, the read address 22 is generated simultaneously in a normal operating state, and so on. The most significant bit in the binary coded addresses changes its level only twice during an address cycle. These changes occur at a first address transition, which occurs at the transition between addresses twenty-one and twenty-two, when the most significant bit passes from a low to a high level, and at a second address transition, one half address-cycle later, at the transition between the addresses forty-three and zero, when the most significant bit in the binary coded addresses passes from a high to a low level (see Figure 3). The first signal $(msb_{wa})_{inv}$ received on the first input 24 of the phase detector derives from the level of the most significant bit on generated write addresses. However, the first signal $(msb_{wa})_{inv}$ also corresponds to the inverted level, since it has passed through the inverting circuit 27. The second signal msb_{ra} corresponding to the actual level of the most significant bit of generated read addresses is received on the second input 26 of the phase detector. In the normal state, in which write and read addresses are generated with a phase shift of one half of an address cycle, the first and the second signal switch from a low to a high level simultaneously, since the first signal is inverted. In a normal state, the phase detector thus receives corresponding level changes from low to high levels in the incoming signals simultaneously, once with each address cycle. The corresponding level changes in the most significant bits in generated read and write addresses are thus received simultaneously in the normal state, i.e. when incoming frames solely contain a nominal number of datainformation units and the write-in rate does not therefore deviate from the nominal write-in rate. On the other hand, corresponding level changes in incoming signals to the phase detector are received with a time shift when the write-in rate has been changed, so that write addresses and read addresses are generated with a shift which deviates from one half of an address cycle. The phase detector 23 delivers to the lowpass filter LP time difference signals td which relate to the time difference between corresponding level changes in the signals arriving at the phase detector 23. A mean time value is derived from consecutive time differences td in the lowpass filter. The mean time value thus forms a mean value of deviations from the normal state between generated write addresses and generated read addresses. The lowpass filter LP deliver to the voltage controlled oscillator VCO a control signal CO obtained from the derived mean time values, so as to adjust the frequency at which clock pulses cl are delivered from the oscillator VCO and therewith either increase or reduce the rate at which read addresses are generated.

Datainformation $DATAINFO_{out}$ is read wordwise from the memory 10 at the rate at which the read addresses are generated. The memory data outputs 16 are connected to inputs 28 on a parallel/series-converter P/S which series converts the datainformation read wordwise from the memory and delivers the information on an output 29 in outgoing frames $Data_{out}$.

Thus, the phase detector 23 of the known arrangement compares a predetermined first address transition in the sequence of write addresses directly with a predetermined number of second address tran-

sitions in the sequence of read addresses. These address transitions differ by one half address cycle, so as to occur simultaneously when the write-in rate is nominal. When a change occurs in the write-in rate and said rate therewith deviates from the nominal rate as earlier described, the address transitions will occur at a given time difference which results in an increase or a decrease in the frequency at which clock pulses c1 are generated, therewith to adjust the read-out rate in keeping with the changed write-in rate. As beforementioned, this momentary change in the read-out rate will result in jitter, for instance. Consequently, an advantage is afforded when using instead an inventive arrangement to transmit datainformation from an SDH-system to a PDH-system when datainformation is divided on frames in accordance with the new standard for 155 MHz-signals, or in some similar manner.

Figure 4 illustrates an embodiment of an inventive arrangement for transmitting datainformation from a SDH-system to a PDH-system. Datainformation DATAINFO$_{in}$ and other information OTHER occurring in the SDH-system is divided on frames Data$_{in}$ in accordance with the above description made with reference to Figure 1. The arrangement illustrated in Figure 4 includes essentially an addressable memory FIFO into which datainformation is written and from which datainformation is read, a write address generator WADRGEN, a read address generator RADRGEN, a detecting means DM for establishing a change in the rate at which datainformation shall be written into the memory, a first derivating means KOMP1, a second derivating means KOMP2, an activating means LC and a phase locking circuit PLL for regulating the rate at which information is read from the memory, so that the read-out rate will, on average, be equally as high as the rate at which information is written into the memory FIFO.

The addressable memory FIFO delimits the SDH-system from the PDH-system and is used for intermediate storage of datainformation DATAINFO$_{in}$ when transmitting data between the two systems. The memory FIFO includes forty-four eight-bit register or memory positions, each of which has a separate address. The memory has eight data inputs 40 for receiving simultaneously the parallel information of eight bits, eight data outputs 41 for delivering the parallel information of eight bits, six write address inputs 42 and six read address inputs 43.

The write address generator WADRGEN includes a write address counter which counts forwards forty-four six-bit binary write addresses WADR between zero and forty-three at cyclicly repeated intervals. Each write address corresponds to the address of one memory position in the memory FIFO. The memory includes forty-four memory positions, since this number is sufficient for the application concerned. The write address generator WADRGEN is provided with six outputs 44 on which the generated write addresses WADR are delivered to the write address inputs 42 on the memory FIFO, wherein datainformation is written into the FIFO-register at the address disclosed on the write address inputs 42. Incoming write clock pulses WCLP are applied to a write pulse input 45, and the write address counter generates a new write address WADR for each write clock pulse, this write address being produced on the outputs 44.

The read address generator RADRGEN includes a six-bit counter which counts forward forty-four binary read addresses RADR between zero and forty-three at cyclicly repeated intervals, which are the same as those for the write addresses. The read address generator RADRGEN is provided with six outputs 46 on which generated read addresses RADR are delivered to the read address inputs 43 on the memory FIFO, wherein datainformation is read-out from the FIFO-register address disclosed on the read address inputs 43. Read clock pulses RCLP are delivered to a read pulse input 47, and the read address counter generates a new read address RADR for each read clock pulse received, this new read address being produced on the output 46.

The detecting means DM is comprised of a Demapper circuit and has eight data inputs 48 for receiving simultaneously the bits in a word of datainformation DATAINFO$_{in}$ or other information OTHER, and also has eight data outputs 49 for delivering simultaneously the bits of a word datainformation DATAINFO$_{in}$ that is to be written into the memory FIFO for further transmission to the PDH-system. The data outputs 49 are connected to the data inputs 40 of the memory. The detecting means DM is also provided with a first and a second control output 50, 51 for delivering control information concerning the write-in and the read-out of datainformation into and from the memory. The second control output 51 is connected to the write pulse input 45 on the write address generator WADRGEN, for delivering write clock pulses WCLP to the write address generator. A write clock pulse is delivered for each word that is to be written into the memory.

The first deriving means KOMP1 includes a first comparison means, or comparator. The deriving means KOMP1 includes nine first inputs 52 to which a first reference address $\underline{a}$ comprising nine bits is applied. On nine second inputs 53 there is applied a comparison address $\underline{b}$ which is comprised of the same write address WADR as those supplied to the memory FIFO and three modulo-8-bits. The first reference address $\underline{a}$ is compared in the first comparator with the comparison address $\underline{b}$ and a comparison magnitude $\underline{x}$ is delivered on an output 54, this comparison magnitude having the form of a write signal pulse xpls when agreement is found between the first reference address $\underline{a}$ and the comparison address $\underline{b}$. The comparison magnitude $\underline{x}$ is comprised of a signal

having a constant level, except when interrupted by a write signal pulse.

The second deriving means KOMP2 includes a second comparison means or a second comparator. Stored in the second comparator KOMP2 is a second reference address c which comprises six bits. A second comparison address d, which is comprised of the same read addresses RADR as those delivered to the memory FIFO, is delivered to six first inputs 55. The second reference address c is compared in the second comparator with the second comparison address d and there is delivered on an output 57 a second comparison magnitude y which when similarity is found between the second reference address c and the second comparison address d is comprised of a read signal pulse ypls. The second comparison magnitude y is comprised of a signal whose level is constant, except when the signal is broken by a read signal pulse ypls.

The activating means LC includes a logic circuit having nine outputs 58 which are connected to the input 52 of the first comparator KOMP1, for delivering the first reference address a to the first comparator KOMP1. The activating means is also provided with an input 59 which is connected to the first control output 50 for receiving a detection signal DET from the detection signal DM. The activating means LC receives from the detection circuit, via the detection signal DET, information which discloses a change in the rate at which datainformation $DATAINFO_{in}$ is written into the memory FIFO.

The phase locking circuit PLL includes a phase detector PD, a lowpass filter LP, and a voltage controlled oscillator VCO. The phase detector has a first input 70 connected to the output 54 on the first comparator KOMP1 for receiving the first comparison magnitude x. The phase detector also has a second input 71, which is connected to the output 57 on the second comparator KOMP2 for receiving the second comparison magnitude y. The phase detector PD functions to detect when, in time, the first comparison magnitude x is comprised of a write signal pulse xpls and when, in time, the second comparison magnitude is comprised of a corresponding read signal pulse ypls, and to detect the time difference between corresponding write signal pulses xpls and read signal pulses ypls. A time difference signal td which contains information concerning the detected time difference between corresponding write signal pulse xpls and read signal pulse ypls is delivered on output 72 of the phase detector. The lowpass filter LP has an input 73 connected to the output 72 of the phase detector, for receiving the time difference signal td. There is derived in the lowpass filter LP a mean value of the time differences between consecutive corresponding write signal pulses and read signal pulses received in the time difference signal td. A control signal co which contains control information is delivered on an output 74 of the lowpass filter LP to the voltage controlled oscillator VCO. This control information depends on the mean values of the time differences between corresponding write signal pulses and read signal pulses derived in the lowpass filter. The voltage controlled oscillator VCO has an input 75 on which the control signal co is received. The voltage controlled oscillator VCO produces on an output 76 a clock signal cl which includes clock pulses having a frequency which is dependent on the control information in the control signal co. The voltage controlled oscillator VCO delivers clock pulses which may thus vary in frequency. The rate of the clock pulses varies around a nominal frequency which corresponds to the nominal rate at which datainformation $DATAINFO_{in}$ occurs in the SDH-system.

In addition to the means already described, the inventive arrangement also includes means for writing datainformation into the memory FIFO and for reading datainformation therefrom.

For datainformation read-in purposes, the inventive arrangement also includes a series/parallel converter 80 and a modulo-8-counter 81. The series/parallel converter 80 has a data input 82 on which earlier described frames $Data_{in}$ containing serial datainformation $DATAINFO_{in}$ and other information OTHER are received. The information contained in the frames $Data_{in}$ arrives at a rate of 155 Mb/s. The information contained in the frames $Data_{in}$ is converted in parallel wordwise and is delivered wordwise from the series/parallel converter 80 on eight data outputs 83 connected to corresponding data inputs 48 on the detection circuit DM. The modulo-8-counter 81 controls the series/parallel converter in a manner such that the information contained in the frames $Data_{in}$ which enter the series/parallel converter 80 serially, will be delivered on the outputs 83 in words of eight bits. The modulo-8-counter 81 has an input 84 on which clock pulses clp having the frequency of 155 MHz are applied. The incoming clock pulses clp are also applied to a second input 85 on the series/parallel converter. The clock pulses clp have the same frequency as, and are fully synchronous with the information contained in the frames $Data_{in}$. The counter 81 includes three binary bits which are counted forwards from the value zero to the value seven at cyclicly repeating intervals in eight steps. The counter steps forward one step for each incoming clock pulse clp. The counter 81 has a first output 86 on which the level of the most significant bit msb is delivered to a third input 87 on the series/parallel converter. The level of the most significant msb passes from a high to a low level once with each eighth clock pulse clp and this is utilized in the parallel conversion, since each word contains eight bits. Eight bits, corresponding to one word, of information are written from the frames $Data_{in}$ into a register in the series/parallel converter. One bit at a time is written into the register over the duration of one clock pulse clp. The most significant bit msb passes

from a high to a low level at each eighth clock pulse clp and the parallel information in the eight-bit register is then transmitted to the detection circuit DM via the outputs 83. The three bits in the modulo-8-counter are delivered on three data outputs 88 connected to three of the second inputs 53 on the first comparitor KOMP1. The three bits delivered by the modulo-8-counter constitute the three least significant bits in the first comparison address b.

For the purpose of reading-out datainformation from the memory FIFO, the inventive arrangement includes a parallel/series converter 90 and a further modulo-8-counter 91. The modulo-8-counter has a clock pulse input 92 connected to the output 76 on the voltage controlled oscillator VCO, for receiving the clock pulses cl from the oscillator. The counter 91 has three binary bits and counts from zero to seven with cyclic repetition. The counter is stepped forwards one step with each clock pulse cl and the counter 91 delivers the aforesaid read clock pulse RCLP on an output 93 with each eighth clock pulse. The parallel/series converter 90 has eight data inputs 94 connected to the data outputs 41 on the memory FIFO for receiving wordwise datainformation $DATAINFO_{out}$ read-out from the memory FIFO. The parallel/series converter 90 has a second input 95 connected to the output on the counter 91, for receiving read clock pulses RCLP. A momentary read address is generated for each read clock pulse RCLP and the word datainformation $DATAINFO_{out}$ which is stored at the momentary address is read-out from the memory to the parallel/series converter 90. The information $DATAINFO_{out}$ read-out from the momentary address is stored intermediately in an eight-bit register in the parallel/series converter 90. The parallel/series converter 90 has a third input 96 connected to the input 92 of the counter, for receiving the clock pulses cl which control the rate at which information is read-out from the memory FIFO. With each clock pulse cl received, the eight-bit register delivers intermediately stored datainformation $DATAOUT_{out}$ bitwise from the parallel/series converter on a data output 97. The datainformation $DATAOUT_{out}$ read-out from the register is divided in frames $Data_{out}$ and is transmitted further in the PDH-system on an outgoing line 98. The rate at which the datainformation occurs in the PDH-system varies around the nominal rate 140 Mb/s.

The inventive arrangement operates in the following manner. Frames $Data_{in}$ containing serial datainformation $DATAINFO_{in}$ and other information OTHER arrives at the series/parallel converter 80 in the SDH-system. The information in the frames $Data_{in}$ is parallel converted in the aforedescribed manner and is delivered wordwise to the detection circuit DM.

The detection circuit DM decodes the information OTHER in each occurring frame $Data_{in}$, so as to establish whether or not the frame contains a nominal number of datainformation units according to Figure 1a or more datainformation units than this nominal number, according to Figure 1b, or fewer datainformation units than nominal, according to Figure 1c. The other information units OTHER in a frame therefore contain information which discloses whether or not the frame contains a nominal number of datainformation units $DATAINFO_{in}$, or fewer datainformation units than the nominal number or more datainformation units than the nominal number. For instance, two bits in the other information OTHER may disclose the number of datainformation units in the frame. 00 discloses that the frame contains a nominal number of datainformation units. 01 indicates that the frame contains more datainformation units than is nominal and 10 denotes that the frame contains fewer datainformation units than is nominal. Each datainformation unit $DATAINFO_{in}$ incoming to the detection circuit DM shall be written into the memory FIFO for further transmission to the PDH-system. To this end, the detection circuit therefore delivers a write clock pulse WCLP to the write address generator WADRGEN for each word of datainformation received. In practice, the detection circuit DM delivers the write clock pulse signal WCLP when it has received a group of eight-bit datainformation. It is not necessary for these bits to derive from one and the same datainformation word, but may derive from two words. This is because other information OTHER may be incorporated bitwise in the datainformation $DATAINFO_{in}$. The write address counter counts forward the next momentary write address WADR in the cyclic sequence with each write clock pulse WCLP received, and when the write address counter delivers the momentary address on the outputs 44, a word comprising eight bits of datainformation is written into the memory position having the corresponding address. Thus, this write-in procedure generates successively a cyclic sequence of write addresses WADR in a manner such that a new write address is generated for each datainformation word to be written into the memory while the generation of write addresses is interrupted with each other information word OTHER. In this way, there is generated a nominal number of write addresses with each frame when a frame having a nominal number of words passes through the detection circuit, and more write addresses are generated per frame than the nominal number when a frame containing more datainformation words than is nominal passes through the detection circuit, and correspondingly fewer write addresses are generated per frame than is nominal when a frame having fewer datainformation words than nominal passes through the detection circuit. Figures 5a-5c illustrate the generation of write addresses in these three separate cases. The vertical axis shows the number of write addresses WADR that are generated in one address cycle. The horizontal axis shows time t. A frame, or more correctly the

part of a frame relevant to the present invention, includes 258, 261 or 264 datainformation words which are to be written into the memory. Since an address cycle contains only 44 addresses, several cycles of write addresses WADR are generated for each frame. Figures 5a-5c illustrate respectively three different cases of the generation of write addresses WADR and interruption in the generation of write addresses.

Figure 5a illustrates the generation of write addresses WADR when the occurrent frame $Data_{in}$ contains a nominal number of datainformation words $DATAINFO_{in}$. Several cycles of write addresses WADR are generated prior to time t_0. The first address in the address cycle is generated at time t_0. The generation of write addresses is interrupted between the time points t_1 and t_2. This interruption extends over that period of time in which a nominal number of other information words OTHER are received in the detection circuit. The last write address in the address cycle is generated at time point t_3.

Figure 5b illustrates the generation of write addresses WADR when the occurrent frame $Data_{in}$ contains more datainformation words $DATAINFO_{in}$ than is nominal. Several cycles of write addresses WADR are generated prior to time t_0. The first address in the address cycle is generated at time t_0. Between the time points t_1 and t_4, the generation of write addresses is interrupted for a period of time which is shorter than the interruption made in Figure 5a. The interruption extends over that period of time in which a fewer number of other information words OTHER than is nominal are received in the detection circuit DM. The last write address in the address cycle is generated at time point t_5, prior to time point t_3 in Figure 5a. Since the interruption, or pause, in Figure 5b is shorter than the interruption in Figure 5a, the addresses in the address cycle which includes this interruption are generated in a shorter space of time in Figure 5b than in Figure 5a. In other words, write addresses WADR are generated at a higher rate between the time points t_0 and t_5 in Figure 5b than between the time points t_0 and t_3 in Figure 5a.

Figure 5c illustrates the generation of write addresses WADR when the occurrent frame $Data_{in}$ contains fewer datainformation words $DATAINFO_{in}$ than is nominal. Several cycles of write addresses WADR are generated prior to time t_0. The first address in the address cycle is generated at time t_0. Between the time points t_1 and t_6, there is made a longer pause in the generation of write addresses than the pause made in Figure 5a. This pause extends over the time in which several other information words OTHER than nominal are received in the detection circuit DM. The last write address in the address cycle is generated at time point t_7, after time point t_3 in Figure 5a. Since the pause in Figure 5c is longer than the pause in Figure 5a, the addresses in the address cycle which contains the pause are generated over a longer period of time in Figure 5c than in Figure 5a. In other words, the rate at which write addresses WADR are generated is slower between the time points t_0 and t_7 in Figure 5c than between the time points t_0 and t_3 in Figure 5a.

Thus, write addresses WADR are generated in the inventive arrangement in the manner described with reference to Figures 5a-5c. The Figures also illustrate how the rate at which the write addresses are generated can vary around the nominal rate illustrated in Figure 5a. Datainformation $DATAINFO_{in}$ is delivered wordwise from the detection circuit DM to the data inputs 40 on the memory FIFO and are written wordwise into the memory FIFO in memory positions disclosed by the write addresses WADR on the write address inputs 42 of the memory FIFO. This write-in of datainformation takes place in conjunction with the generation of a momentary write address WADR.

Read addresses RADR are generated continuously, without interruption, when reading datainformation $DATAINFO_{out}$ from the memory FIFO. The rate at which the addresses are generated, however, may vary so as to follow the rate at which write addresses WADR are generated. The same memory addresses as the memory addresses in the cyclic sequence of write addresses are included in the sequence of read addresses and in the same order. Datainformation $DATAINFOOUT_{out}$ is read wordwise from memory positions in the memory FIFO disclosed by the read addresses RADR on the read address inputs 43 of the memory FIFO.

Figure 6 illustrates the continuous generation of read addresses RADR and also shows how the generation rate varies. The illustrated rate variations are greatly exaggerated. The vertical axis shows the read addresses RADR of one address cycle. The horizontal axis shows time t. All forty-four addresses in an address cycle are generated during the time period A, between the time points t_0 and t_1, at a nominal rate, which takes place when write addresses are generated at the nominal rate in accordance with the Figure 5a illustration. During the next time period B, between the time points t_1 and t_2, the read addresses RADR in the address cycle are generated at a higher rate than the nominal rate, which takes place when the write addresses WADR are generated at a higher rate than the nominal rate, in the manner shown in the Figure 5b illustration. On the other hand, the read addresses RADR in the address cycle are generated at a slower rate than the nominal rate during the time period C, between the time points t_2 and t_3, which takes place when the write addresses WADR are generated at a lower rate than the nominal rate, as shown in the Figure 5c illustration.

Thus, the memory FIFO is used for writing-in and reading-out datainformation simultaneously. Certain memory positions are used for writing-in information at the same time as other memory positions are used

for reading-out information. Consequently, parallel write addresses WADR and read addresses RADR are generated for writing-in and reading-out datainformation. However, it is highly essential that the momentary addresses in the sequence of write addresses are considerably shifted from the momentary addresses in the sequence of read addresses when generating said addresses. This is to eliminate the possibility of datainformation being written into and read from the memory at the same memory positions simultaneously. In an ideal state, a starting state, the read addresses are generated with a phase shift of one-half address cycle from the simultaneously generated write addresses. In practice, however, a momentary mean value AVWADR of consecutive write addresses is generated in the starting state phase shifted through one-half cycle from corresponding momentary read addresses RADR. The mean value of generated write addresses is used because the generation of write addresses is not continuous, but includes the aforedescribed interruption. In the starting state, generated write addresses will therefore vary around a write address mean value AVWADR which is shifted through one-half address cycle from corresponding read addresses RADR.

Figure 7 illustrates an addressable memory FIFO. The "cake slices" in the memory shown in Figure 7 illustrate the memory positions with associated addresses. An upper arrow illustrates a momentary mean write address value AVWADR, while a bottom arrow illustrates a simultaneous, momentary read address RADR. The momentary mean write address value AVWADR and corresponding, simultaneous read addresses RADR are phase shifted through one-half of an address cycle in relation to one another in the Figure 7 illustration. The two arrows are continuously displaced clockwise subsequent to the generation of new write addresses and read addresses. Provided that the write addresses and the read addresses are generated at mutually the same rate, the momentary mean write address value AVWADR and a momentary, simultaneous mean read address value RADR will be displaced mutually through one-half of an address cycle. When the write-in rate increases as a result of the frames in the SDH-system containing more datainformation units $DATAINFO_{in}$, the rate at which write addresses WADR are generated will also increase. This can be illustrated in Figure 7 by shifting the momentary mean write address value AVWADR clockwise in the drawing, as shown by a third arrow D, thereby reducing the phase difference between the momentary mean value address AVWADR and corresponding read address RADR. When the write-in rate decreases, because the frames occurring in the SDH-system contain fewer datainformation units $DATAINFO_{in}$, the rate at which write addresses WADR are generated will also decrease. This can be shown in Figure 7 by displacing the momentary mean write address value AVWADR clockwise, in the direction shown by a fourth arrow E, wherewith the phase difference between the momentary mean value address AVWADR and corresponding read address RADR will decrease.

It is the intention of the invention to adjust the read-out rate to the write-in rate, such that the phase shifts between momentary read addresses RADR and the simultaneous, momentary mean write address values AVWADR are continuously adjusted back to the starting state after a phase shift from said starting state. The phase shift between momentary read addresses RADR and simultaneous, momentary mean write address values AVWADR deviate from one-half of an address cycle when there is no agreement between the write-in rate and the read-out rate, although this phase shift will return to one-half of an address cycle when the read-out rate is adjusted to be equally as high as the write-in rate. Thus, the inventive arrangement functions to ensure that, on average, the read-out rate will be equally as high as the write-in rate and, therewith, also that the read addresses RADR are generated, on average, at the same rate as the write addresses WADR.

The first reference address $\underline{a}$ comprising nine binary bits is formed in the logic circuit in the activating means. The reference address $\underline{a}$ is variable. The six most significant bits correspond to a write address. The three least significant bits are used to denote eighths of the write addresses. In the starting state, the first reference address $\underline{a}$ is assigned the value zero, corresponding to the write address zero, wherein all nine bits denote the value zero. The first reference address $\underline{a}$ is transmitted from the activating means LC to the first derivation means KOMP1 and stored therein. The second reference address $\underline{c}$ comprising six binary bits which correspond to a write address is stored permanently in the second comparitor or derivation means KOMP2. In the starting state, the second reference $\underline{c}$ is assigned the value twenty-two. The mutual phase shift of the reference addresses a, c in the starting state therewith corresponds to the phase shift between a momentary mean write address value AVWADR and corresponding momentary read addresses RADR in the starting state, i.e. a shift of half an address cycle.

The first comparitor KOMP1 receives the second comparison address $\underline{b}$, which includes the momentary write addresses WADR and three modulo-8-bits from the modulo-8-counter 81. The first reference address $\underline{a}$ is compared continuously in the comparitor KOMP1 with the first comparison address $\underline{b}$ and the result of the comparison denotes the first comparison magnitude x. When the comparison shows similarity between the addresses a, b, a write signal pulse xpls is sent from the comparitor KOMP1 to the phase detector PD in the phase-locking circuit PLL. In the starting state, a write signal pulse xpls is delivered

when the write address WADR and the three modulo-8-bits from the counter 81 are zero. This will therefore occur once with each write address cycle. The second comparitor KOMP2 receives the second comparison address d, which includes the momentary read addresses RADR. The second reference address c is compared continuously in the comparitor KOMP2 with the second comparison address d, and the comparison result denotes the second comparison magnitude y. When the comparison shows agreement between the second addresses c, d, a read signal pulse ypls is sent from the comparitor KOMP2 to the same phase detector PD. In the starting state, a read signal pulse ypls is transmitted when the read address RADR twenty-two is generated. This therefore occurs once with each read address cycle. The write signal pulses xpls are generated, on average, at the same time as the read signal pulses ypls in the starting state of the system, since the phase shift between momentary read addresses RADR and corresponding momentary mean write address values AVWADR correspond to the mutual phase shift of the reference addresses a, c, as illustrated in Figure 8.

Figure 8 illustrates the write and read signal pulses xpls, ypls delivered by said comparitors KOMP1, KOMP2 when write addresses WADR and read addresses RADR are generated in the starting state of the system. The respective vertical axes x and y correspond to the first and the second comparison magnitudes. The horizontal axes show time t. The comparison magnitudes have a low level, except when the aforesaid pulses are generated. The lower diagram shows read signal pulses ypls that are generated at time points t_0, t_1, t_2 and t_3. The four read signal pulses are generated during four mutually sequential address cycles, and since the read addresses RADR are generated continuously, the read signal pulses ypls will occur at a constant time interval T between the pulses, in the starting state of the system. The read signal pulses ypls are generated when the read address twenty-two is generated in the read address generator RADRGEN. The time period between the generation of the read addresses RADR twenty-two in a sequence of address cycles will therefore be constant. Since the write addresses WADR are not generated continuously, but disrupted with pauses, the write signal pulses xpls will, on average, only be generated at the same time as corresponding read signal pulses ypls in the starting state of the system. Thus, corresponding momentary read signal pulses and write signal pulses will not be generated exactly simultaneously with one another, but that a momentary write signal pulse xpls will occur at a given time shift in relation to a corresponding momentary read signal pulse. The upper diagram in Figure 8 shows momentary write signal pulses xpls and corresponding momentary read signal pulses ypls. The write signal pulses xpls occur at time points t_{00}, t_{11}, t_{22} and t_{33} in four mutually sequential address cycles. The momentary read signal pulse ypls occurring at time point t_0 has a corresponding write signal pulse xpls which occurs at time point t_{00}, the read signal pulse ypls occurring at time point t_1 has a corresponding write signal pulse xpls at time point t_{11}, and so on. It will be seen from the Figure that the write signal pulses xpls occur before the corresponding read signal pulse ypls in two instances and that the write signal pulses occur after corresponding read signal pulses in another two instances. However, the sequence of write pulses xpls shown in the Figure occur, on average, at the same time as the corresponding sequence of read addresses ypls. Thus, in the starting state of the system, a sequence of momentary write signal pulses xpls is generated, on average, at the same time as the corresponding momentary read signal pulses ypls.

Figures 9a and 9b show that momentary write signal pulses xpls are, on average, generated with a time shift in relation to corresponding read signal pulses ypls, when the phase shift between momentary read addresses RADR and corresponding mean write address values AVWADR differ from the phase shift between the reference addresses a, c as a result of an increase or a decrease in the rate at which datainformation is written-in.

Figure 9a illustrates when the write signal pulses xpls occur in relation to corresponding read signal pulses ypls at a slower write-in rate. The write signal pulses xpls will then occur later in comparison with the write signal pulses xpls in the Figure 8 illustration, meaning that the write signal pulses xpls in the Figure 9a illustration are shifted to the right in comparison with the write signal pulses in the Figure 8 illustration. The write signal pulses in the Figure 9a illustration occur at the time points t_{0+}, t_{1-}, t_{2+} and t_{3+}. Thus, on average, the write signal pulses xpls occur later than the corresponding read signal pulses ypls when the write-in rate decreases.

Figure 9b illustrates the case when the write signal pulses xpls occur in relation to corresponding read signal pulses ypls at a higher write-in rate. The write signal pulses xpls then occur earlier than the write signal pulses xpls in the Figure 8 illustration, which means that the write signal pulses xpls in Figure 9b are shifted to the left in comparison with the write signal pulses in Figure 8. The write signal pulses in Figure 9b occur at the time points t_{0-}, t_{1-}, t_2 and t_{3-}. Thus, on average, the write signal pulses xpls occur earlier than the corresponding read signal pulses ypls when the write-in rate increases.

The write signal pulses xpls and the read signal pulses ypls are received in the phase detector PD which detects the time difference between a received write signal pulse xpls and corresponding read signal pulse. Information concerning detected time differences is sent to the lowpass filter LP, which derives

a mean value from detected time differences. The time differences diff0, diff1, diff2 and diff3 are detected in Figure 8. The average time difference is calculated to zero in the lowpass filter from these values, which means that the rate at which read addresses are generated is equally as high as the rate at which write addresses are generated, which in turn means that the rate at which read addresses RADR are generated shall not be changed. The control signal co to the voltage controlled oscillator VCO will then contain information to the effect that the rate of the clock pulses cl shall be kept constant. On the other hand, if average time difference exists, positive or negative, the control signal co will contain information to the effect that the rate of the clock pulses cl shall be changed.

In the example illustrated in Figure 9a, the time differences diff0+, diff2+ and diff3+ are detected instead. There is calculated in the lowpass filter from these values a mean positive time difference, which signifies that write addresses are generated at a slower rate than the rate at which read addresses are generated. This implies that the read address generating rate shall be lowered. The control signal co will then contain information to the effect that the clock pulse rate cl shall be lowered, so that read addresses and write addresses are generated at mutually the same rate.

In the example illustrated in Figure 9b, the time differences diff0-, diff1- and diff3- are detected instead. There is calculated in the lowpass filter from these values a mean negative time difference which signifies that the write address generating rate is higher than the rate at which read addresses are generated. This implies that the rate at which read addresses are generated shall be increased. The control signal co will then contain information to the effect that the clock pulse rate cl shall be increased, so that read addresses and write addresses will be generated at mutually the same rate.

In order to control the adjustment of clock pulses cl from the voltage controlled oscillator VCO, there is first established a change in the number of datainformation words in incoming frames $Data_{in}$. This corresponds to establishing a change in rate in the generation of write addresses. The generation rate change is established with the aid of the detection circuit DM which in each incoming frame $Data_{in}$ reads the two bits in the other information OTHER which denote whether the number of datainformation units in the frame is nominal, greater than nominal or smaller than nominal. When the number of datainformation words is greater or smaller than nominal, this indicates that there is a change in rate. When a rate change is established in the detection circuit, the rate change is masked initially for the phase detector PD, by changing the first reference address a to an extent which corresponds to the detected change. Masking is effected by changing the first reference address a in a manner which corresponds to the detected change in the number of incoming datainformation words. Information concerning detected changes in the number of datainformation words in incoming frames $Data_{in}$ is delivered to the activating means, i.e. the logic circuit LC, with two binary bits in the signal DET. The signal DET may include three different kinds of information. In a first case, the signal indicates that the first reference address a shall be changed in a positive direction to the same extent as the detected change. This takes place when the incoming frame $Data_{in}$ includes three datainformation units more than is nominal. For instance, if the reference address a is zero, the address shall be changed to three. In a second case, the first reference address a shall be changed in a negative sense by three addresses. This takes place when the incoming frame $Data_{in}$ includes three datainformation units fewer than is nominal. For instance, the reference address a is then changed from zero to forty-one. In the third case, the first reference address is left unchanged. This occurs when the incoming frame $Data_{in}$ contains a nominal number of datainformation units.

By changing the first reference address a in a manner which corresponds to the detected change in the rate at which write addresses are generated in the aforedescribed manner, the mutual phase shift between the two reference address a, c is changed to a value which is equally as large as the mean phase shift between generated write addresses and read addresses as a result of the detected rate change. As a result of the change of the reference address a, i.e. the mask, the write signal pulses xpls are not shifted from the read signal pulses in the manner illustrated in Figures 9a and 9b, and the write signal pulses xpls will occur, on average, at the same time as the read signal pulses ypls, despite the change in the rate at which write addresses WADR are generated. Masking is effected so that the phase-locking circuit PLL will not react immediately to the whole of the rate change that has been detected. As a result of the mask, the phase-locking circuit PLL will not "detect" immediately the change in the write-in rate, since the first reference address a is compensated for the changed write-in rate.

After masking the reference address a, or compensating said reference address, it remains to adjust the read-out rate to a value which is equal to the write-in rate. According to the present invention, this adjustment is effected in several steps.

The read-out rate is adjusted, by finally restoring the first reference address a successively to said starting state. In the case of the illustrative embodiment, this means that the first reference address a is changed back to zero in incremental steps. During this stepwise return of the reference address a to the starting state, the write signal pulses xpls will, on

average, be generated with a time shift in relation to corresponding read signal pulses ypls. This will result in an adjustment of the readout rate, since the phase detector PD will receive write signal pulses xpls and read signal pulses ypls with a mean time difference, in the manner described with reference to Figures 9a and 9b. During this readjustment period, the phase detector PD receives write signal pulses and read signal pulses with small mean time differences, which results in small successive changes in the read-out rate until said rate is equally as high as the write-in rate.

Hitherto, and for the sake of simplicity, changes in the first reference address a, masking and readjustment, have been described as being effected by changing the reference address a solely in steps or increments which include complete addresses. However, an important feature of the invention is that the reference address a can also be changed in steps which are smaller than complete addresses. The first reference address may be divided into eight parts in each address, so that masking and readjustment can be effected in steps in which each step corresponds to one-eighth of the full address. To this end, the three least significant bits in the first reference address are used to denote one-eighths of complete addresses. The six most significant bits denote complete addresses. A comparison is made in the first comparitor KOMP1 between the reference address a and the comparison address b, and in order to enable the comparison to be made on a bit level, the comparison address b also includes nine bits. The three least significant bits in the comparison address b from the modulo-8-counter 81 enables the comparison to be made on a bit level. The three least significant bits in the comparison address are counted eight times for each write address WADR in the comparison address b.

In practice, the reference address a is not changed exactly by three addresses when masking the reference addres a, but is changed short of three addresses, or more precisely is changed by two and six-eighths of the addresses. Thus, the most significant bits are given the binary address two and the least significant bits are given the binary value six. Thus, each address can be divided into eight parts having mutually different binary values between 000, 001, ..., 111, through the agency of the three least significant bits. The reason why the change is short of three addresses instead of being precisely three addresses, is because the SDH-system and the PDH-system have different bit rates. The time taken to transmit twenty-four bits of information in the SDH-system is equal to the time taken to transmit twenty-two bits in the PDH-system, since the rate is lower in the PDH-system than in the SDH-system. Thus, when changing the rate in the SDH-system, the corresponding change in the PDH-system is masked.

The readjustment can also be carried out in eighths of a step with the aid of the three least significant bits in the first reference address a. It is preferred to carry out the readjustment in eighths of a step of complete addresses. When the reference address a has the binary value two and six-eighths addresses and shall be adjusted back in eighths of a step, the readjustment is thus carried out in twenty-two steps before the reference address a has been returned to the value zero.

The reference address a is masked in one single step, wherein said first reference address a is changed through a corresponding number of addresses as the detected change in the number of datainformation words in incoming frames $Data_{in}$. The return of the reference address is effected successively, wherein the read-out rate is adjusted. It may happen that a new masking is carried out before the preceding masking has had time to reduce. Consequently, the first reference address a may deviate by more than three addresses from the starting state and must therefore be readjusted at different speeds, depending on the extent in which it deviates from the starting state.

Figure 10 is a diagram which illustrates those addresses that the first reference address a can assume. The reference address a is equal to zero in its starting state. According to the illustrated embodiment, the reference address a can be permitted to vary by fifteen addresses in a forwards sense and fifteen addresses in a rearward sense in relation to the address zero. The deviation from the starting state should not be greater than said fifteen addresses, because otherwise there is a risk that a given write address WADR will be generated at the same time as the same read address RADR, since the generation of write addresses is displaced in the diagram in the same manner as the reference address a is displaced when changing the write-in rate. The reference addresses are divided into five different sectors in the Figure 10 illustration. The first sector K includes the addresses 39-6, i.e. those addresses proximal to the starting state. The second and the third sector L include the addresses 36-38 and 7-9. The deviation of the addresses in the L-sectors is further from the starting state than the addresses in the K-sector. The fourth and the fifth sectors M include the addresses 30-35 and 10-15. The addresses in the M-sectors deviate most from the starting state, when compared with the K-sectors and the L-sectors. The readjustment of the reference address a is effected at different speeds, depending on the sector in which the reference address is found. When the reference address a has a value within the K-sector, the readjustment is effected at a slower rate, meaning, for instance, that the reference address a is changed back towards the starting state at one-eighth of an address at a time, and each adjustment takes place relatively seldomly. On the other hand, if the reference address has a val-

ue within one of the L-sectors, the address is readjusted at a faster rate, for instance at a rate corresponding to one-eighth of an address at a time, but relatively often. Finally, when the reference address has a value within one of the M-sectors, readjustment is effected very quickly, so as to avoid the reference address from being located outside the limit addresses 15 and 30. In this case, the reference address can be readjusted in eighths of a step of addresses and very often. In order to readjust the reference address with sufficient speed, it is possible to readjust in greater steps than eighths of addresses, or even at a speed corresponding to one complete address in one step. The readjustment of the first reference address a is effected and controlled by the logic circuit LC.

It is preferred to use only the first reference address a for compensating for a change in the write-in rate, although it is also possible to use instead the second reference address c or to use both reference addresses a, c together for the purpose of compensation. Changes are made in the reference address c by connecting nine additional outputs 60 on the logic circuit to nine additional inputs 56 on the second comparitor KOMP2. In order to be able to make changes on parts of addresses, three modulo-8-bits are also transmitted to the second comparitor KOMP2 from the modulo-8-counter 91. The three bits that are received on three inputs 61 constitute the three least significant bits in the second comparison address d. When only the second reference address c is used for compensation, the address c is varied around the starting state in a manner which corresponds to the earlier described changes to the first reference address a. When both reference addresses a, c are used together to mask a change in the write-in rate, they are together changed by a total number of addresses which equals the change in the number of datainformation units in the incoming frame $Data_{in}$. The readjustment may involve adjusting both reference addresses a, c alternately back to the starting state.

It will be understood that the invention is not restricted to the aforedescribed and illustrated exemplifying embodiments thereof. For instance, the invention can be applied in a context in which the number of datainformation units in a frame can vary in a way different to that described hitherto, for instance such that the datainformation units $DATAINFO_{in}$ contain two or four more units than the nominal number, or two or four datainformation units $DATAINFO_{in}$ less than the nominal number. Naturally, the other information OTHER must contain more than two bits in order to indicate this.

The invention can also be applied in contexts in which the number of datainformation units $DATAINFO_{in}$ or predetermined changes in the rate at which write addresses are generated/delivered is detected in a manner different to that earlier described. When practicing the invention, it is important that the changes in the rate at which write addresses are delivered to the memory is of a predetermined nature and can be detected/determined in time for the initial compensation. Of course, purely random changes cannot be masked with an initial compensation according to the present invention.

Neither is the invention restricted to precisely the type of phase detector described, but can be applied together with other types of known phase detectors.

Claims

1. A method for adapting the rate at which a cyclic sequence of read addresses (RADR) is delivered to a memory (FIFO) to the rate at which a cyclic sequence of write addresses (WADR) is delivered to said memory, wherein the sequence of write addresses is delivered at a rate which is changed intermittently to a predetermined extent, and wherein the rate at which the read addresses are delivered to the memory is adjusted in a manner such that the read addresses will be delivered to the memory, on average, at the same rate as that at which the write addresses are delivered to said memory, **characterized** by establishing a change in the rate at which the write addresses are delivered to the memory; deriving a first comparison magnitude (x) from the write addresses and a second comparison magnitude (y) from the read addresses; comparing the first and the second comparison magnitudes; adjusting the rate at which the read addresses are delivered to the memory in accordance with the result (co) of said comparison, by activating the derivation of at least one of the comparison magnitudes to a predetermined degree which corresponds to the aforesaid predetermined extent, such that at least the major part of the detected change is initially compensated in the derivation of at least one of the comparison magnitudes; and reducing the activation of said derivation successively, so as to reduce the compensation successively.

2. A method according to Claim 1, in which the incoming datainformation to be written into the memory with the aid of the write addresses is divided in frames, wherein the frames also include other information which is not to be written into the memory, and wherein the amount of datainformation contained in a frame may coincide with or deviate from a predetermined nominal value in a predetermined manner, **characterized** by detecting whether or not the quantity of datainformation contained in a frame coincides with or deviates from the nominal value in the predetermined manner, therewith to establish the change in the rate at which write addresses are delivered

to the memory.

3. A method according to Claim 1 or 2, **characterized** by deriving the first comparison magnitude (x) from the write addresses by forming a first reference address (a) which corresponds to a write address; comparing the write address (WADR) delivered to the memory (FIFO) with the first reference address, the result of said comparison forming the first comparison magnitude (x); deriving the second comparison magnitude (y) from the read addresses by forming a second reference address (c) which corresponds to a read address; comparing the read address (RADR) delivered to the memory (FIFO) with the second reference address, the result of said comparison forming the second comparison magnitude (y), wherein the reference addresses (a, c) in a starting state in the absence of said activation are formed with a mutual difference which corresponds generally to one-half cycle phase difference in a sequence of addresses, wherein said first comparison magnitude is comprised of a write signal pulse (xpls) which is generated when the write address is equal to the first reference address, and wherein said second comparison magnitude is comprised of a read signal pulse (ypls) which is generated when the read address is equal to the second reference address, whereby the pulses (xpls, ypls) are generated simultaneously when the phase shift between the read addresses and the simultaneous write addresses corresponds to the phase shift between the reference addresses, whereas said pulses are generated with a time shift when the phase shifts between delivered read addresses and the simultaneous write addresses differ from the phase shift between the first and the second reference addresses.

4. A method according to Claim 3, **characterized** in that the comparison between the first and the second comparison magnitudes (x, y) is effected by comparing when in time the write signal pulses and the read signal pulses (xpls, ypls) generated and adjusting the rate at which new read addresses (RADR) are delivered to the memory (FIFO) in accordance with the result (co) of the comparison, wherein the rate is increased when the write signal pulse (xpls) is generated prior to the read signal pulse (ypls), the rate is decreased when the write signal pulse is generated after the read signal pulse, and the rate is kept unchanged when the write signal pulse and the read signal pulse are generated simultaneously with one another.

5. A method according to Claim 3, **characterized** in that activation of the derivation of at least one of the comparison magnitudes in conjunction with changing the rate at which the write addresses are delivered to the memory is changed to a predetermined extent is effected initially by changing the first reference address (a) or the second reference address (c) or both reference addresses together (a, c) to a degree which corresponds to said predetermined extent; and in that the activation of said derivation is reduced successively by adjusting the changed reference address or reference addresses incrementally in steps back to said starting state while said write signal pulse (xpls) and said read signal pulse (ypls) are generated with a time shift, so that the rate at which read addresses are delivered to the memory is adjusted to follow the changed rate at which write addresses are delivered to the memory, said rate being changed to a predetermined extent.

6. An arrangement for adapting the rate at which a cyclic sequence of read addresses (RADR) is delivered to a memory (FIFO) to the rate at which a cyclic sequence of write addresses (WADR) is delivered to said memory, said sequence of write addresses being delivered at a rate which is changed intermittently to a predetermined extent, wherein the arrangement includes control means (PLL) for adjusting the rate at which the read addresses are delivered to the memory, so that the read addresses, on average, are delivered to the memory at the same rate as the write addresses are delivered to said memory, **characterized** by detecting means (DM) for establishing a change in the rate at which the write addresses are delivered to the memory; first deriving means (KOMP1) for deriving a first comparison magnitude (x) from the write addresses, and second deriving means (KOMP2) for deriving a second comparison magnitude (y) from the read addresses; first comparison means (PD) for comparing the first and the second comparison magnitudes; and further characterized in that said control means (PLL) functions to adjust the rate at which the read addresses are delivered to the memory in accordance with the result (co) of the comparison made in the first comparison means; in that the arrangement further includes activating means (LC) for activating derivation of at least one of the comparison magnitudes (x) to a predetermined degree corresponding to said predetermined extent, so that at least the major part of a preset change is compensated initially when deriving at least one (x) of the comparison magnitudes; and in that the activating means functions to reduce successively the influence of the derivation so that said compensation is reduced successively and ceases as a result of a preset

change.

7. An arrangement according to Claim 6, in which datainformation to be written into the memory with the aid of the write addresses occurs divided in frames, wherein said frames also include other information which shall not be written into the memory, and wherein the amount of datainformation contained in a frame may coincide with a predetermined nominal value or deviate from said value in a predetermined manner, **characterized** in that the detection means (DM) functions to establish the change in the rate at which write addresses are delivered to the memory by detecting whether or not the amount of datainformation in a frame coincides with the nominal value or deviates from said value in said predetermined manner.

8. An arrangement according to Claim 6 or 7, **characterized** in that the first deriving means (KOMP1) includes a first comparitor to which a first reference address (a) is delivered and to which there is also delivered the same write addresses (WADR) as those delivered to the memory (FIFO), wherein said comparitor is intended to compare the first reference address delivered thereto with the write addresses delivered thereto and to deliver said first comparison magnitude (x) in the form of a write signal pulse (xpls) when similarity is found between said reference address and said write addresses; in that said second driving means (KOMP2) includes a second comparitor to which there is delivered a second reference address (c) and the same read addresses (RADR) as those delivered to the memory (FIFO), said second comparitor functioning to compare the second reference address delivered thereto with the read addresses delivered thereto and to deliver said second comparison magnitude (y) in the form of a read signal pulse (ypls) when similarity is found between the second reference address and the read addresses.

9. An arrangement according to Claim 8, **characterized** in that the first comparison means includes a phase detector (PD) which receives the write signal pulse (xpls) on a first input and receives the read signal pulse (ypls) on a second input, said phase detector functioning to detect any time shift between a write signal pulse and a corresponding read signal pulse and to deliver on one output a control signal (co) which is dependent on a detected time shift; in that said control means (PLL) includes a voltage controlled oscillator (VCO) which receives said control signal (co) on one input and delivers on one output a signal having a frequency (f) which determines the rate at which read addresses are delivered to the memory; in that the voltage controlled oscillator (VCO) functions to increase the rate at which new read addresses are delivered to the memory (FIFO) when the write signal pulses are generated prior to the corresponding read signal pulses; in that the oscillator is intended to reduce said rate when the write signal pulses are generated after corresponding read signal pulses; and in that the oscillator is intended to maintain said rate unchanged when corresponding write signal pulses and read signal pulses are generated at one and the same time.

10. An arrangement according to Claim 8, **characterized** in that the activating means (LC) includes a logic circuit which, when establishing a predetermined change in the rate at which the write addresses are delivered, functions to compensate said change; in that the logic circuit is connected to the first comparitor (KOMP1) and is constructed to effect a change in the first reference address (a) corresponding to said predetermined extent, so as to initially compensate the whole of said change; and in that the logic circuit is constructed to remove the change in the reference address (a) in incremental steps, so that the compensation is successively reduced and ceases.

11. A method for transmitting datainformation from a synchronous digital hierarchy system (SDH) to a plesiochronous digital hierarchy system (PDH), said datainformation ($DATAINFO_{in}$) occurring divided on frames in the synchronous system, wherein the frames include units of datainformation ($DATAINFO_{in}$) to be transmitted to the PDH-system, and also units of other information which shall not be transmitted to the PDH-system, wherein the relationship between the number of datainformation units and the number of other information units may vary in each frame, depending on whether the frame includes a nominal number of datainformation units or more datainformation units than the nominal number or fewer datainformation units than the nominal number, and wherein the method includes the steps of writing datainformation ($DATAINFO_{in}$) from the synchronous system into an addressable memory (FIFO) and reading-out datainformation ($DATAINFO_{out}$) to the plesiochronous system from the addressable memory, and in which method a cyclic sequence of write addresses (WADR) is generated successively in a manner such that there is generated one write address for each unit of datainformation ($DATAINFO_{in}$) to be transmitted to the PDH-system, whereas the generation of write addresses is interrupted for each unit of other information, whereby a nominal number of

write addresses are generated for each frame when a frame having a nominal number of datainformation units occurs in the synchronous system, and more write addresses than the nominal number of addresses are generated for each frame when the occurrent frame includes more datainformation units than said nominal number, and fewer write addresses than the nominal number of addresses are generated for each frame when the occurrent frame includes fewer datainformation units than the nominal number, wherein datainformation ($DATAINFO_{in}$) from the synchronous system is written into memory positions in the memory disclosed by the write addresses, wherein a cyclic sequence of read addresses (RADR) are generated, wherein the same memory addresses as the memory addresses included in the cyclic sequence of write addresses are included in the sequence of read addresses and in the same order as said memory addresses, wherein datainformation ($DATAINFO_{out}$) is readout to the plesiochronous system from memory positions in the memory disclosed by the read addresses (RADR), wherein in a starting state, the read addresses are generated generally phase shifted through one-half of an address cycle from the simultaneously generated write addresses, so that data will not be written into and read from the memory simultaneously from one and the same memory position, and in which method the read addresses are generated, on average, at the same rate as the write addresses, **characterized** by

- forming a first reference address (a) which corresponds to a write address, and forming a second reference address (c) which corresponds to a read address, such that the mutual phase shift in the reference addresses (a, c) corresponds essentially to one-half of an address cycle in a starting state;
- generating a write signal pulse (xpls) when the write address (WADR) is equal to the first reference address (a), and generating a read signal pulse (ypls) when the read address (RADR) is equal to the second reference address (c), whereby said pulses (xpls, ypls) are generated mutually simultaneously when the phase shift between the read addresses and the write addresses correspond to the mutual phase shift of the reference addresses, whereas said pulses (xpls, ypls) are generated with a time shift when the phase shift between the read addresses and the write addresses differ from the phase shift between the reference addresses;
- delivering said pulses (xpls, ypls) to a frequency regulating circuit (PLL) which functions to adjust the rate at which new read addresses (RADR) are generated, wherein said rate is changed when the write signal pulse (xpls) and corresponding read signal pulse (ypls) are generated with a mutual time shift, and wherein the rate is unchanged when the write signal pulse (xpls) is generated at the same time as the read signal pulse (ypls);
- detecting when an occurrent frame contains more or more datainformation units ($DATAINFO_{in}$) than the nominal number;
- when detecting that a frame contains more or fewer datainformation units than the nominal number, masking corresponding generation of more or fewer write addresses (WADR) for said frame, by changing the first reference address (a) or the second reference address (c) or both reference addresses together (a, c) by as many reference addresses as the number corresponded by more or fewer datainformation units;
- adjusting the changed reference address or reference addresses (a, c) stepwise back to said starting state, wherein the write signal pulse (xpls) and the read signal pulse (ypls) are generated with a mutual time shift, so that the rate at which read addresses (RADR) are generated is changed to follow the change in the number of write addresses (WADR) generated for each frame which occurs with more or fewer datainformation units than is nominal in a frame, wherein said rate increases when the frame contains more information units and decreases when the frame contains fewer units than the nominal frame number.

12. A method according to Claim 11, **characterized** in that when detecting more datainformation units than the nominal number, it is also detected that one or more first spaces (H3) in the frame intended for transmitting more datainformation units than the nominal number contain datainformation, and when detecting fewer datainformation units than the nominal number, it is detected that one or more other spaces (0) in the frame do not contain datainformation and are not utilized for datainformation when transmitting fewer datainformation units than the nominal number.

13. A method according to Claim 11, **characterized** in that when the incoming frame includes fewer datainformation units ($DATAINFO_{in}$) than the nominal number, the corresponding generation of more write addresses is masked by changing

the first reference address (a) forwards by as many reference addresses as the number of more datainformation units contained in the frame above said nominal number, and when the incoming frame includes fewer datainformation units ($DATAINFO_{in}$) than the nominal number, the corresponding generation of fewer write addresses is masked by changing the first reference address (a) backwards by as many reference addresses as the fewer number of datainformation units contained by the frame in relation to the nominal number.

14. A method according to Claim 13, **characterized** in that masking is effected in one step.

15. A method according to Claim 13, **characterized** by adjusting the first reference address (a) backwards towards the starting state subsequent to effecting said masking operation, wherein

- the deviation of the first reference address (a) from the starting state is measured; and
- the first reference address (a) is adjusted backwards to the starting state in incremental steps at a rate which becomes greater with increasing deviations of the first reference address from the starting state.

16. A method according to Claim 15, **characterized** in that said stepwise adjustment of the first reference address (a) back to the starting state is effected in parts of reference addresses.

17. An arrangement for transmitting datainformation from a synchronous digital hierarchy system (SDH) to a plesiochronous digital hierarchy system (PDH), said datainformation ($DATAINFO_{in}$) occurring divided on frames in the synchronous system, wherein the frames include units of datainformation ($DATAINFO_{in}$) to be transmitted to the PDH-system, and also units of other information which shall not be transmitted to the PDH-system, wherein the relationship between the number of datainformation units and the number of other information units in each frame may vary, depending on whether the frame includes a nominal number of datainformation units or more datainformation units than the nominal number or fewer datainformation units than the nominal number, and in which arrangement datainformation ($DATAINFO_{in}$) from the synchronous system is written into the addressable memory (FIFO) and datainformation ($DATAINFO_{out}$) is read-out to the plesiochronous system from the addressable memory, and which arrangement includes write address generator (WADRGEN) for generating a cyclic sequence of write addresses (WADR) such as to generate one write address for each unit of datainformation ($DATAINFO_{in}$) to be transmitted to the PDH-system, whereas the generation of write addresses is interrupted for each unit of other information, whereby a nominal number of write addresses is generated for each frame when a frame having a nominal number of datainformation units occurs in the synchronous system, and more write addresses than the nominal number of addresses are generated for each frame when the occurrent frame includes more datainformation units than said nominal number, and fewer write addresses than the nominal number of addresses are generated for each frame when the occurrent frame includes fewer datainformation units than the nominal number, wherein datainformation ($DATAINFO_{in}$) from the synchronous system is written into memory positions in the memory disclosed by the write addresses, wherein the arrangement further includes a read address generator (RADRGEN) for generating a cyclic sequence of read addresses (RADR), wherein the same memory addresses as the memory addresses included in the cyclic sequence of write addresses are included in the sequence of read addresses and in the same order as said memory addresses, wherein datainformation ($DATAINFO_{out}$) is read-out to the plesiochronous system from memory positions in the memory disclosed by the read addresses (RADR), wherein in a starting state the read addresses are generated generally phase shifted through one-half of an address cycle from the simultaneously generated write addresses, so that data will not be written into and read from the memory simultaneously from one and the same memory position, and in which arrangement the read addresses are generated, on average, at the same rate as the write addresses, **characterized** in that the arrangement also includes

- a first comparison means (KOMP1) for making a comparison between a first reference address (a) and generated write addresses (WADR), wherein a write signal pulse (xpls) is delivered on an output when the write address is the same as the first reference address;
- a second comparison means (KOMP2) for making a comparison between a second reference address (c) and generated read addresses (RADR), wherein a read signal pulse (ypls) is delivered on an output when the read address is the same as the second reference address;
- a frequency regulating circuit (PLL), having an output connected to said read address generator (RADRGEN) for adjusting the counting rate at which read addresses are generated, receives the write signal pulse

(xpls) on a first input and the read signal pulse (ypls) on a second input, wherein the counter rate is adjusted when the write signal pulse (xpls) and the read signal pulse (ypls) are received with a mutual time shift, whereas the counter rate remains unchanged when the write signal pulse and the read signal pulse are received simultaneously;

- a logic circuit (LC) which is coupled to control the first reference address (a) or is coupled to control the second reference address (c) or is coupled to control both the first reference address (a) and the second reference address (c) simultaneously, wherein the reference addresses in a starting state have a mutual phase shift which corresponds to one-half of an address cycle, wherein said write signal pulse (xpls) and said read signal pulse (ypls) are delivered simultaneously when the phase shift between generated write addresses and simultaneously generated read addresses correspond to the phase shift between said first and said second reference address;
- a detection circuit (DM) for detecting more or fewer datainformation units (DATAINFO$_{in}$) than the nominal number of datainformation units in an incoming frame, wherein the detection circuit (DM) has an output connected to an input on said logic circuit (LC) for delivering a detection signal (DET) to the logic circuit (LC) when detecting more or fewer datainformation units than the nominal number, wherein corresponding generation of more or fewer write addresses is masked for the frequency regulating circuit, by changing in one step the first reference address (a) or the second reference address (c) or both reference addresses (a, c) together by as many reference addresses which correspond to the number of more or fewer datainformation units in said frame, whereafter the changed reference address or reference addresses (a, c) are adjusted in stepped increments back to said starting state while the write signal pulse (xpls) and the read signal pulse (ypls) are generated mutually shifted in time, such that the counter rate at which read addresses (RADR) are generated is changed in a manner to follow the change in the generation of write addresses (WADR) which occurs when the incoming frame contains more or fewer datainformation units than the nominal number, and wherein the frequency regulating circuit (PLL) increases the counter rate as a result of detecting more datainformation units than the nominal number in a frame, and decreases the counter rate as a result of detecting fewer datainformation units in the incoming frame than the nominal number.

18. An arrangement according to Claim 17, **characterized** in that the frequency regulating circuit (PLL) includes a phase-locking circuit having a phase detector (PD) for detecting the mutual time shift of the write signal pulse (xpls) and the read signal pulse (ypls), wherein the phase detector (PD) delivers a control signal (co) which depends on the detected time shift, and further includes a voltage controlled oscillator circuit (VCO) which receives the control signal (co) and adjusts the frequency of a clock signal (cl) in response to the received control signal (co), and a counter (91) which receives the clock signal (cl) and which delivers read-clock pulses (RCLP) to the read address generator (RADRGEN), wherein the read clock pulses are delivered at a frequency which depends on the mutual time shift between the write signal pulse and the read signal pulse, and wherein the counter rate in the read address generator varies with the frequency of the read clock pulses.

19. An arrangement according to Claim 17, **characterized** in that the first and the second comparison means (KOMP1, KOMP2) are comparitors.

20. An arrangement according to Claim 17, **characterized** in that the logic circuit (LC) functions to change the first reference address (a) in a forward sense when detecting more datainformation units in an incoming frame than the nominal number of said units, wherein the reference address is changed in a forward sense by as many reference addresses as the additional number of datainformation units above said nominal number, and wherein the logic circuit functions to change the first reference address (a) in a backward sense when detecting fewer datainformation units, and wherein the reference address is changed in a backward sense by as many reference addresses as the fewer number of datainformation units; and in that the logic circuit (LC) also functions to adjust the first reference address (a) back to the starting state in incremental steps such that the number of steps and the time period between said steps is dependent on the extent to which the first reference address (a) has been changed from said starting state, wherein said adjustment is effected with large steps or at short time intervals between the steps when the reference address deviates to a great extent from said starting state, and is effected in small steps

and with long time intervals between said steps when the reference address deviates from said starting state by only a small extent.

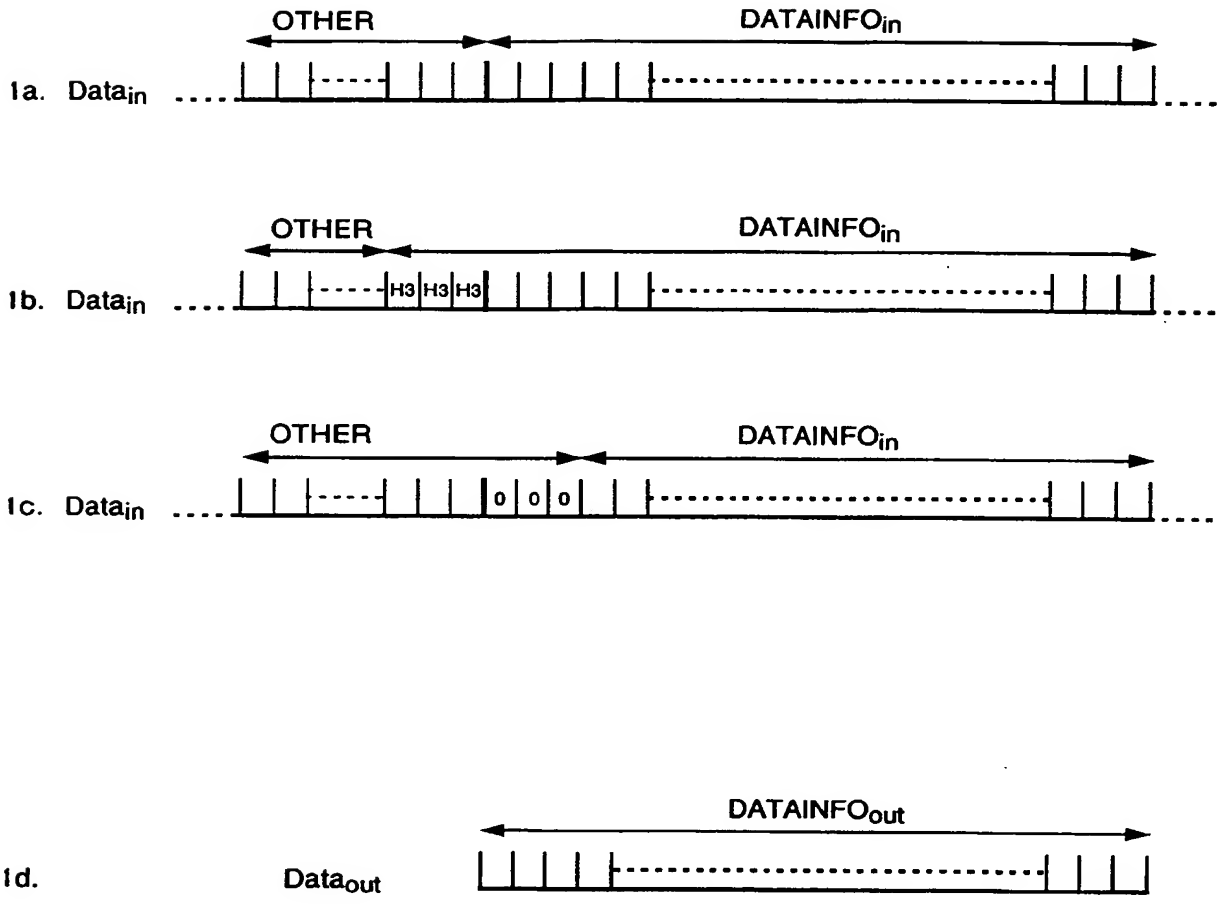

Fig. 1

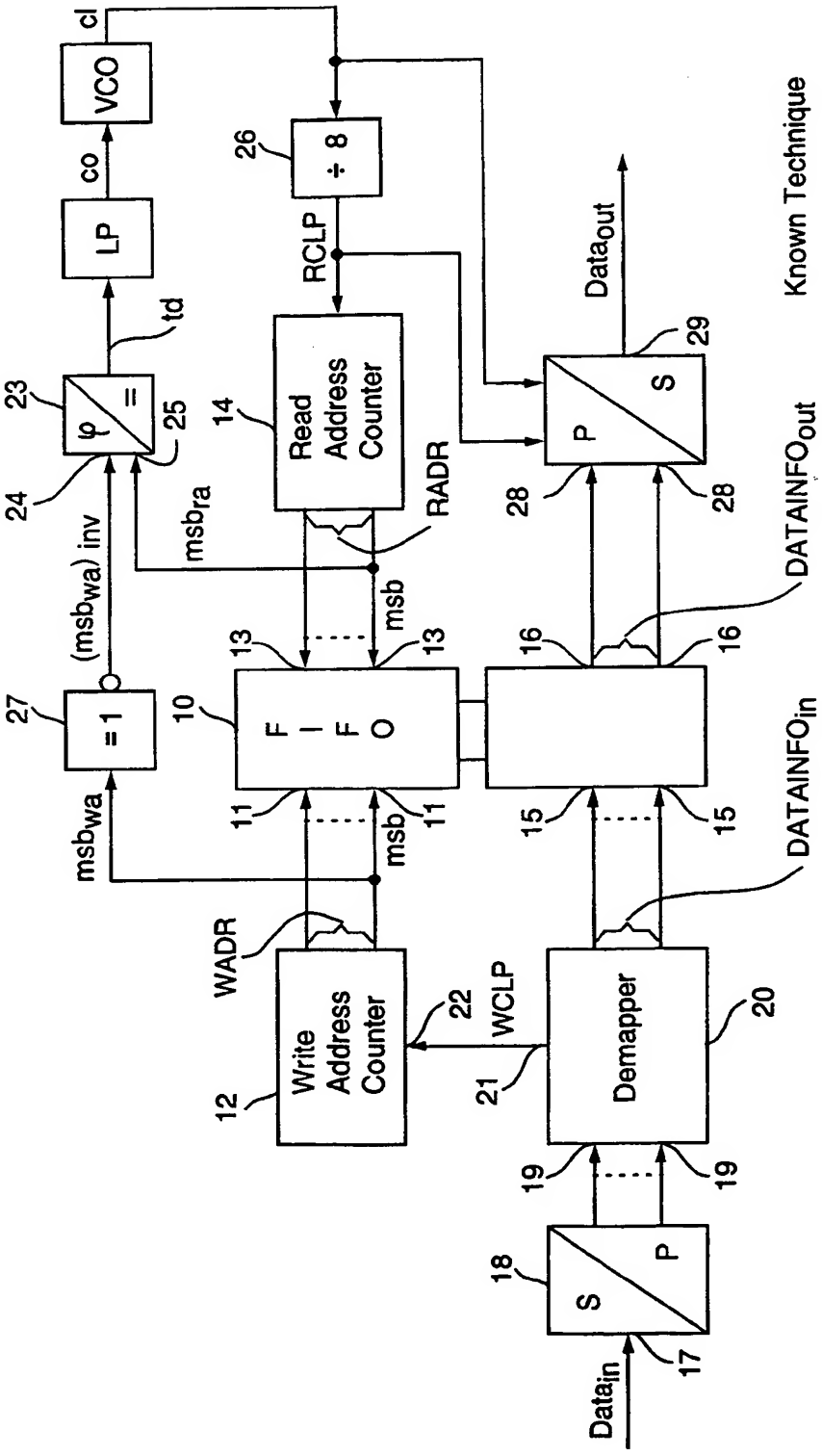
cl
VCO
co
LP
td
23
φ
=
25
24
msb_wa inv
msb_ra
27
= 1
msb_wa
26
÷ 8
RCLP
14
Read Address Counter
RADR
msb
13
13
10
F — F O
11
11
msb
WADR
12
Write Address Counter
22
WCLP
21
Demapper
20
19
19
18
S
P
17
Data_in
Data_out
29
P
S
28
28
16
16
DATAINFO_out
15
15
DATAINFO_in
Known Technique

Fig. 2

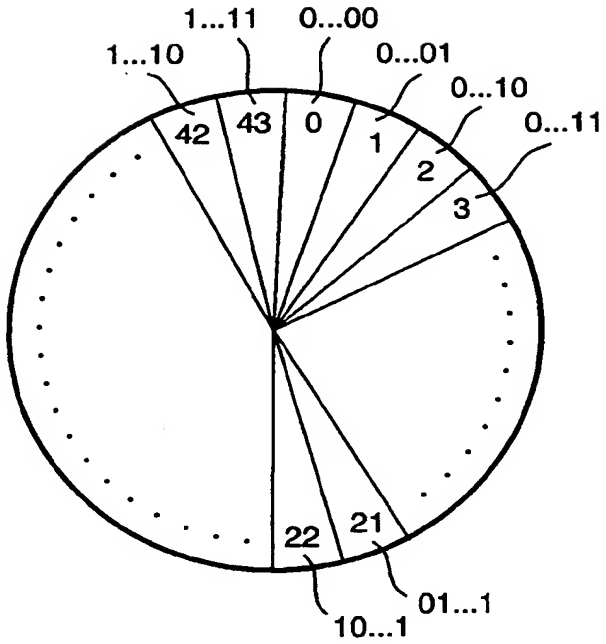

Fig. 3

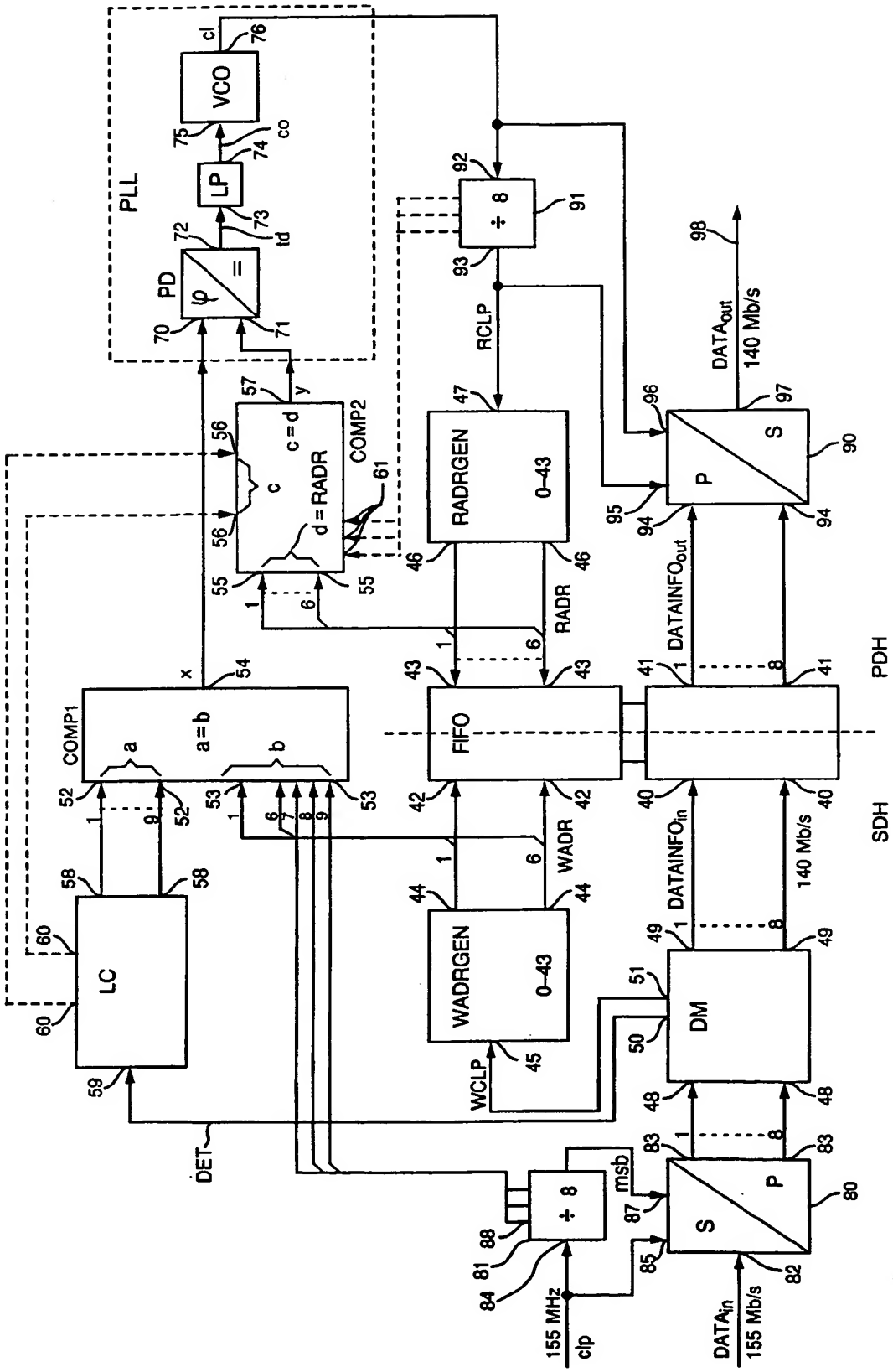
PLL
VCO
LP
PD
÷ 8
RADRGEN
0–43
WADRGEN
0–43
COMP1
a
a=b
b
COMP2
c
c=d
d=RADR
FIFO
LC
DM
P
S
RCLP
RADR
WADR
WCLP
DET
msb
DATAout
140 Mb/s
DATAINFOout
DATAINFOin
140 Mb/s
155 MHz
clp
DATAin
155 Mb/s
PDH
SDH

Fig. 4

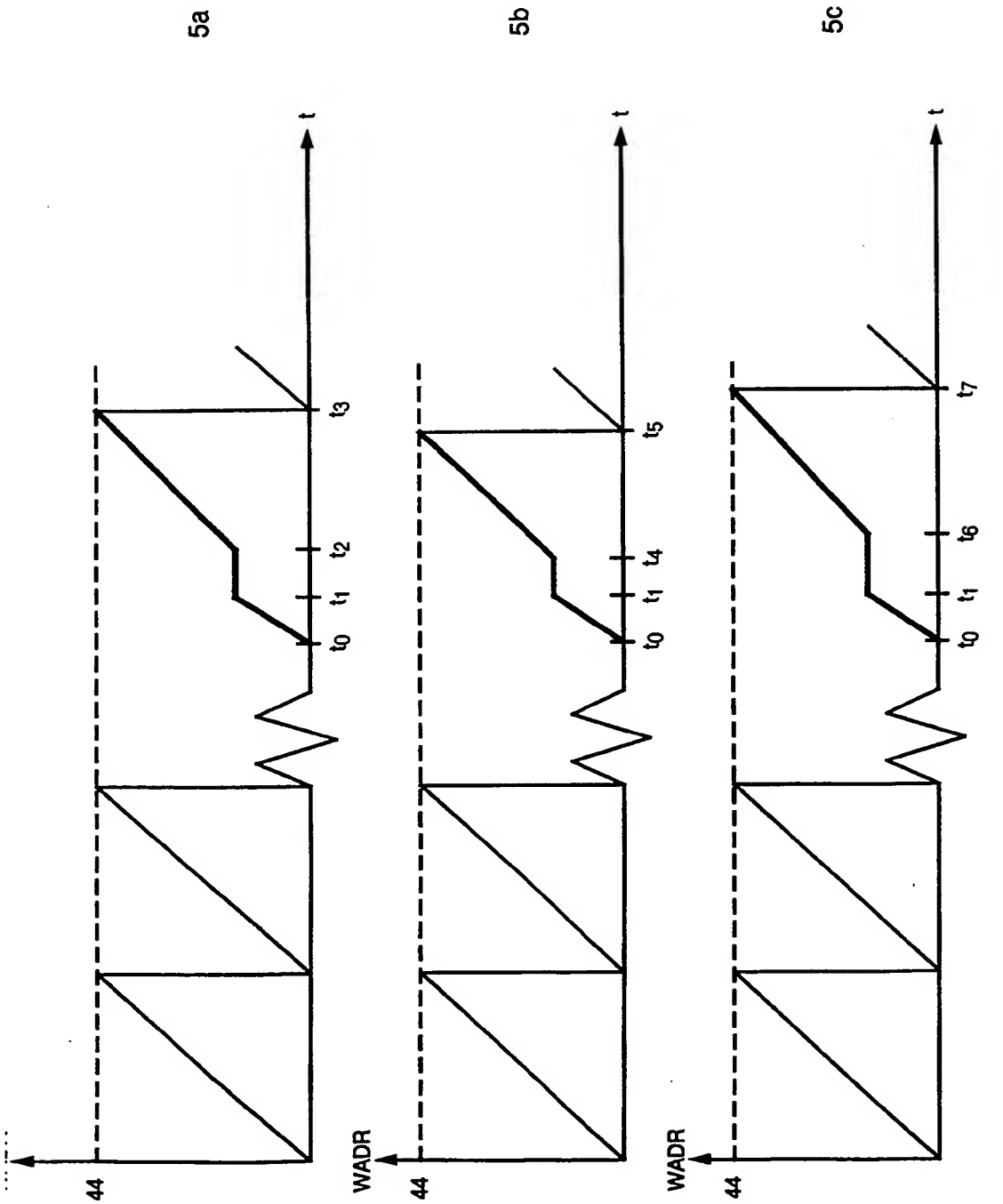

Fig. 5

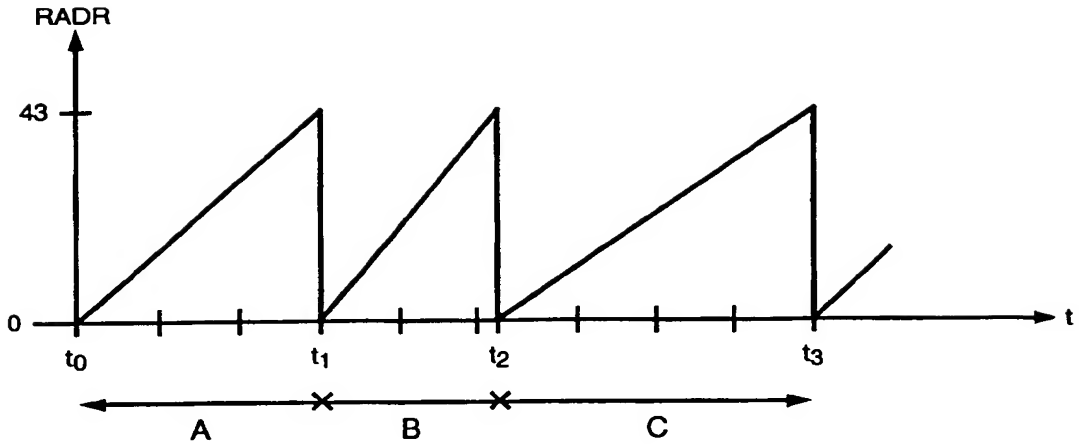

Fig. 6

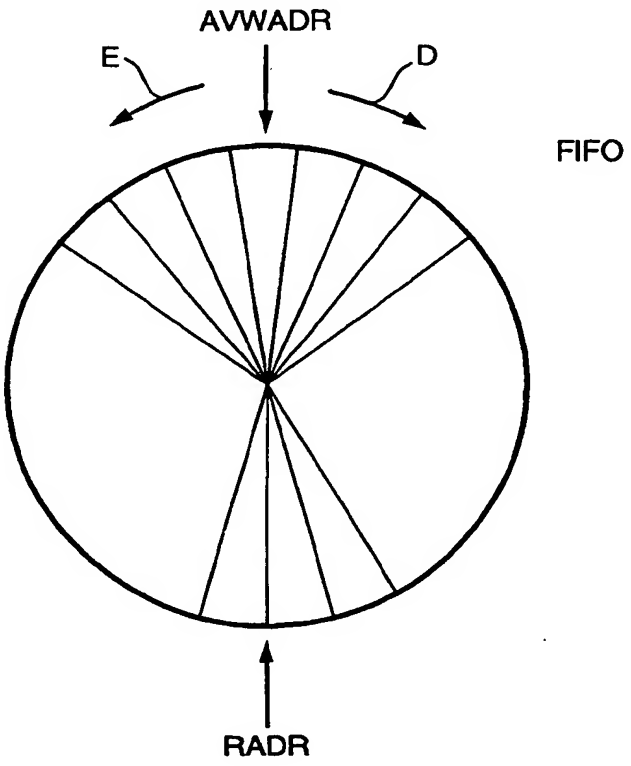

Fig. 7

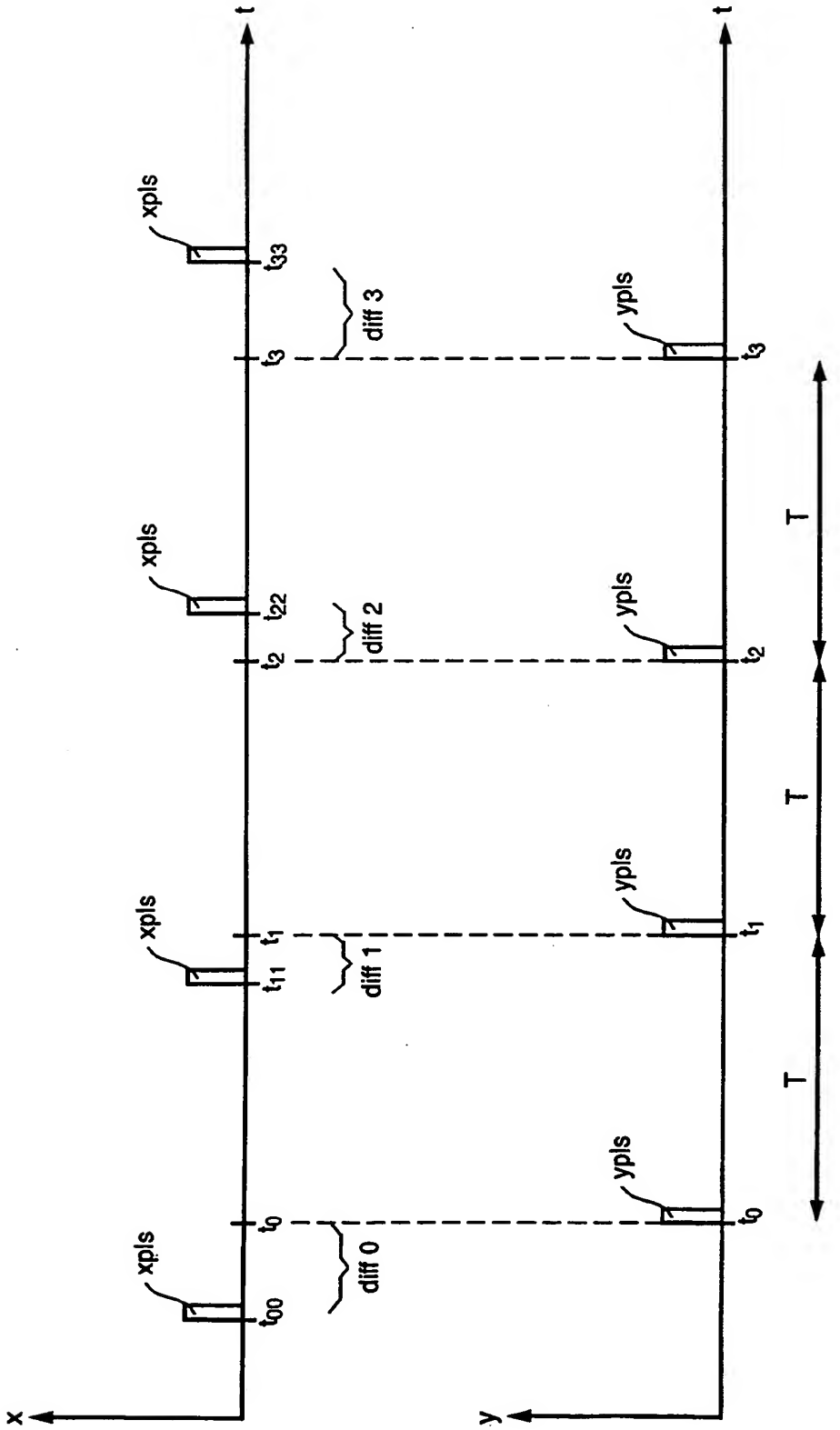
t
xpls
t_{33}
diff 3
t_3
ypls
t_3
xpls
t_{22}
diff 2
t_2
ypls
t_2
T
xpls
t_{11}
t_1
diff 1
ypls
t_1
T
xpls
t_{00}
t_0
diff 0
ypls
t_0
T
x
y

Fig. 8

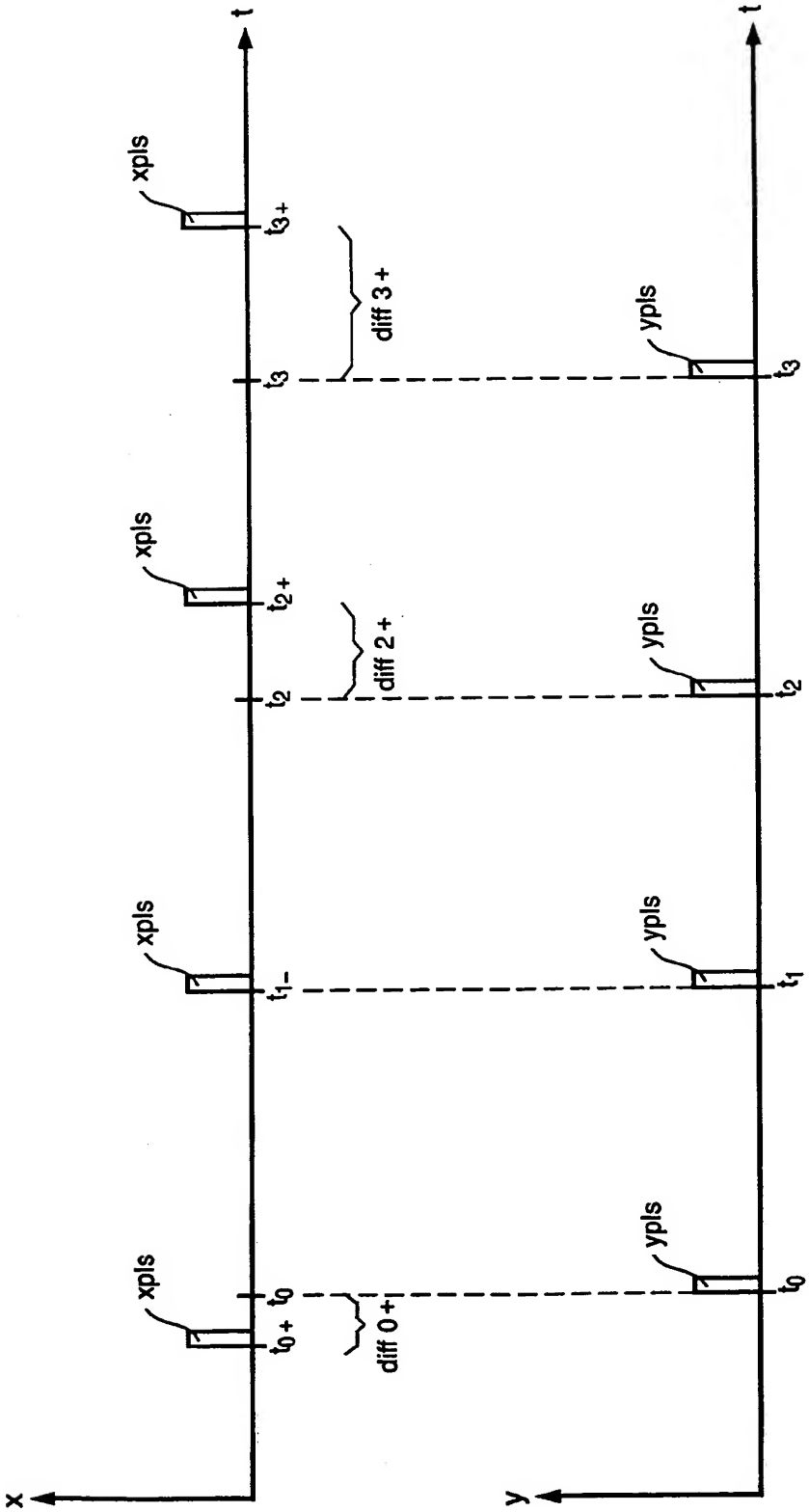
t
xpls
t_{3+}
diff 3 +
t_3
ypls
t_3
xpls
t_{2+}
diff 2 +
t_2
ypls
t_2
xpls
t_{1-}
ypls
t_1
xpls
t_0
t_{0+}
diff 0 +
ypls
t_0
x
y

Fig. 9a

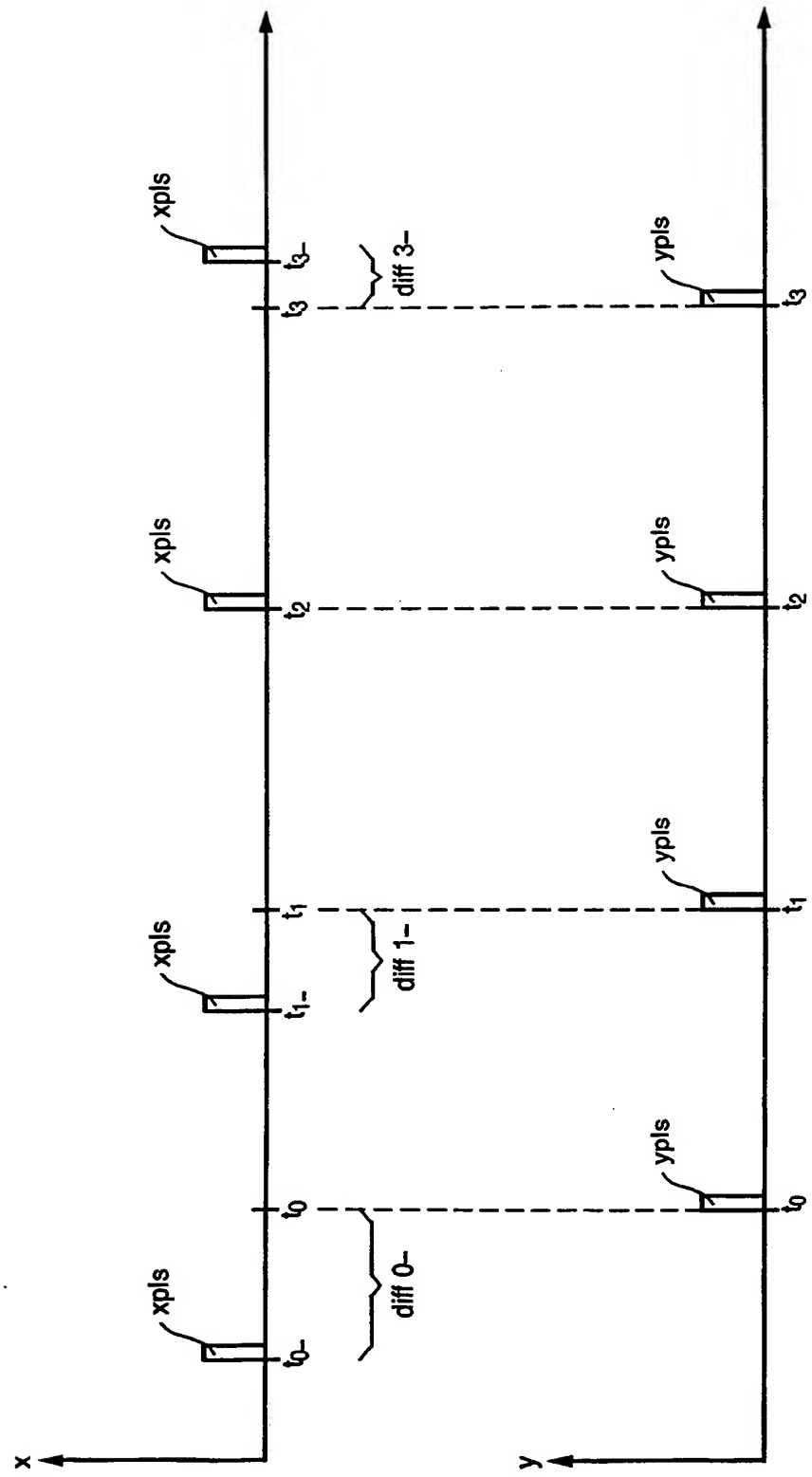

Fig. 9b

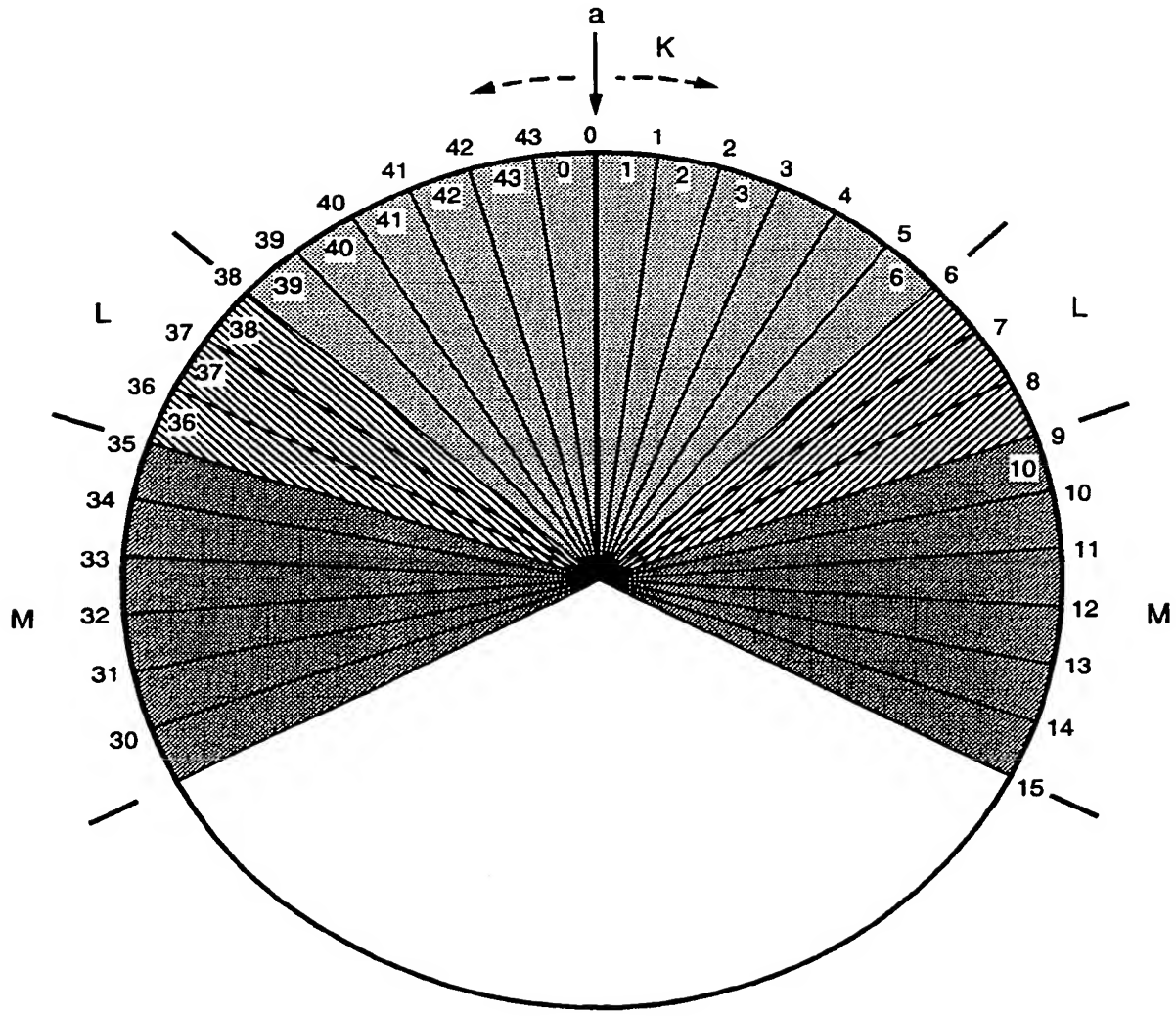
a
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Fig. 10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP93850104.6

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 941 156 (KENNETH J. STERN ET AL) *Column 1, line 60 - column 2, line 37; figure 7*	1-20	H04J 3/07 G06F 5/06
A	EP-A2-0 475 497 (PHILIPS PATENT-VERWALTUNG GMBH) *figure 1; abstract*	1-20	
A	US-A-5 052 025 (DONALD G DUFF ET AL) *column 1, line 53 - column 2, line 22; figure 1*	1-20	
A	US-A-4 884 286 (ANDRE SZCZEPANEK ET AL) *abstract*	1-20	
A	EP-A2-0 292 208 (AMERICAN TELE-PHONE AND TELEGRAPH COMPANY) *figure 5; abstract*	1-20	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H04J H04L G06F
A	WO,A1, 8 807 300 (ANTONIO CANTONI ET AL) *abstract*	1-20	
A	EP-A2-0 459 686 (AMERICAN TELEPHO-NE AND TELEGRAPH COMPANY) *abstract; figure 1*	1-20	
A,P	EP-A2-0 507 385 (PHILIPS PATENT-VERWALTUNG GMBH) *figure 7; abstract*	1-20	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
STOCKHOLM	23-08-1993	FREDRIKSSON. K

EPO FORM 1503 03.82 (P0401)

CATEGORY OF CITED DOCUMENTS

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